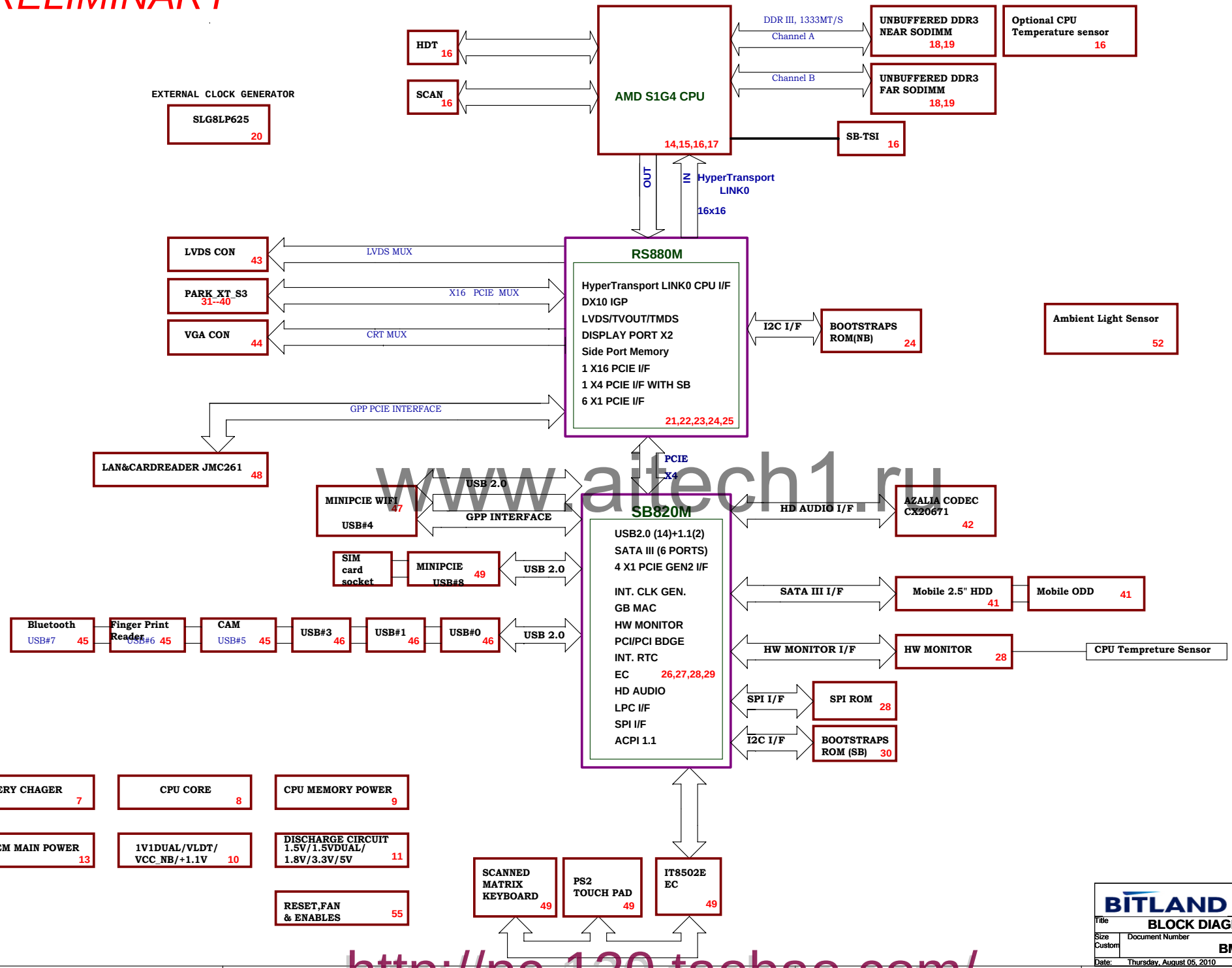
PRELIMINARY

GUAM S1G4 SCHEMATIC DESIGN



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Notebook R&D Division

Title	BLOCK DIAGRAM	
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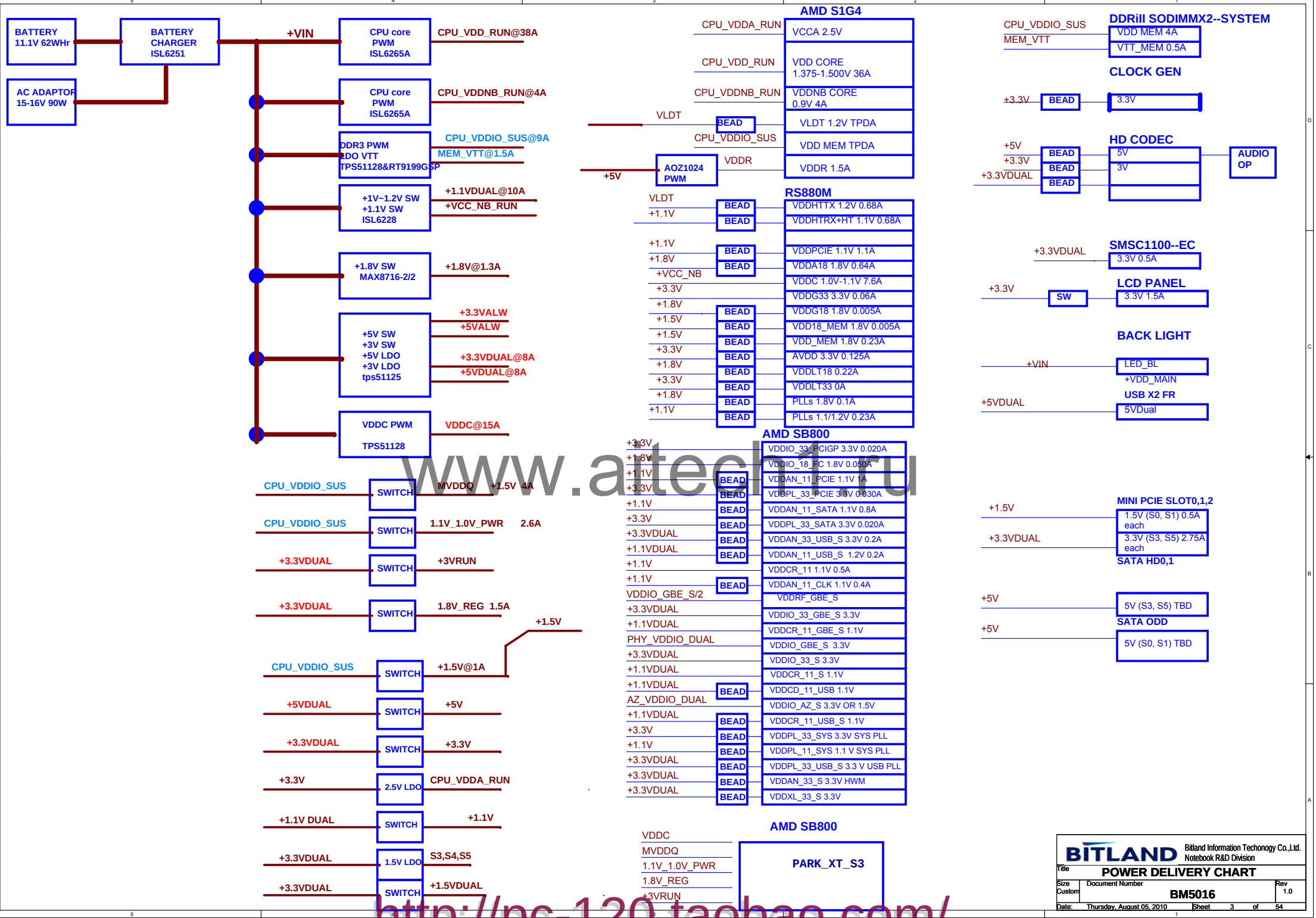
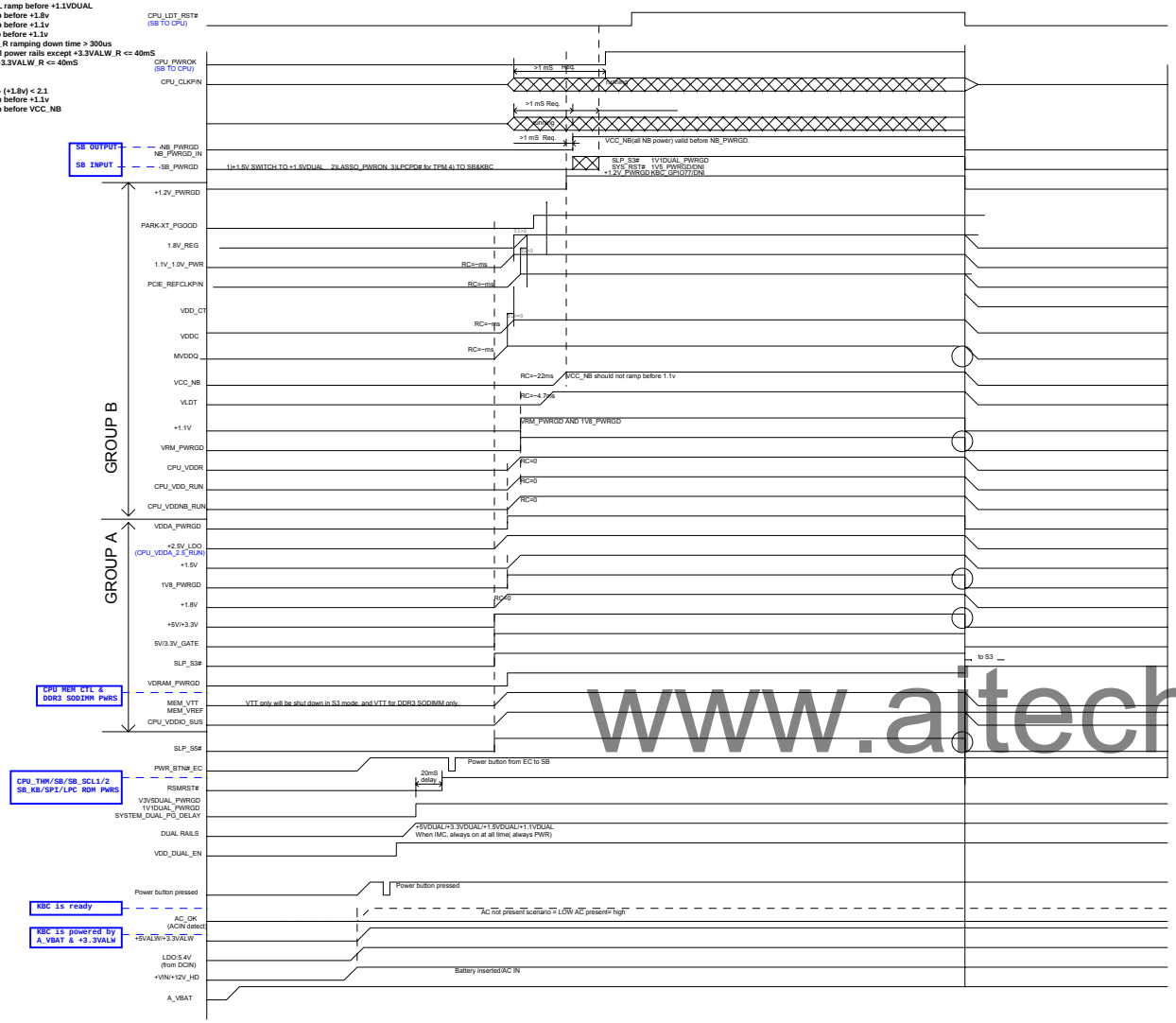


Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



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Title: POWER SEQUENCE CHART

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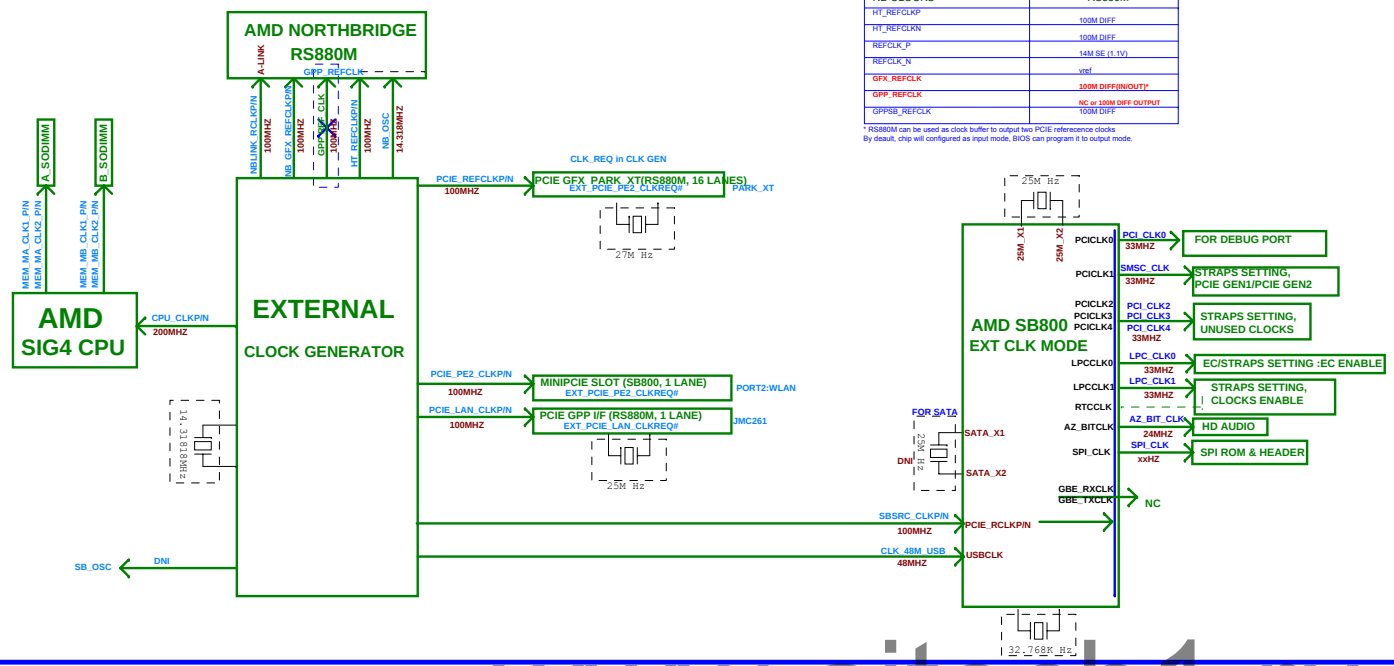
EXTERNAL CLOCK MODE

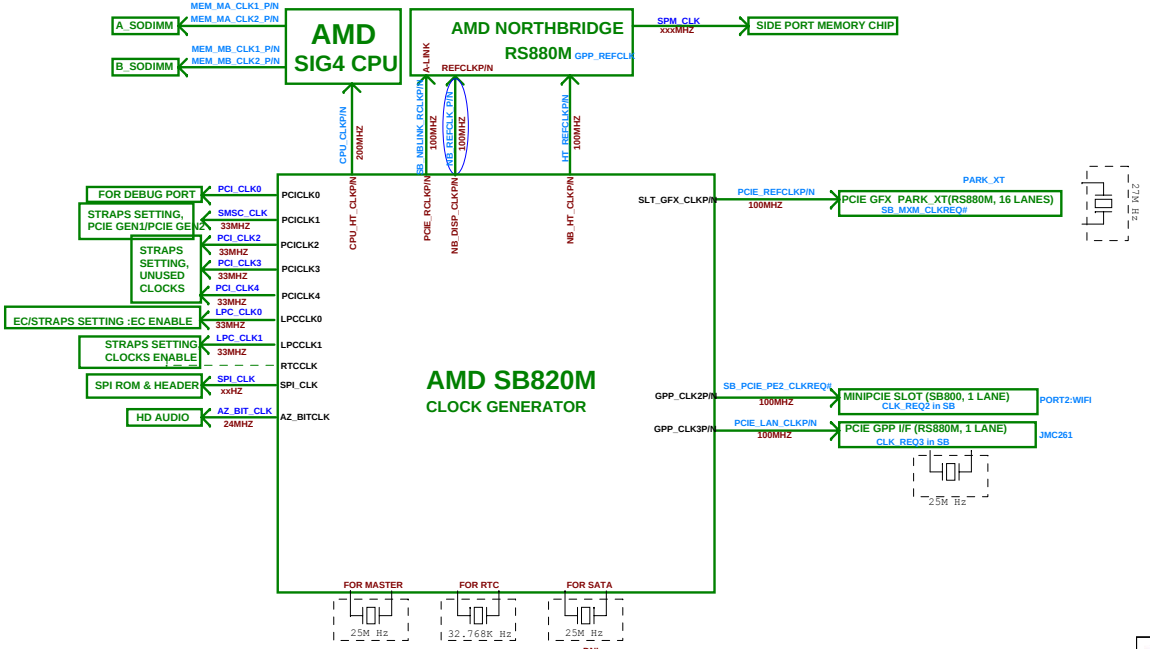
NB CLOCK INPUT TABLE

NB CLOCKS	RS880M
HT_REFCLKP	100M DIFF
HT_REFCLKN	100M DIFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	vref
GFX_REFCLK	100M DIFF(IN/OUT)*
GPP_REFCLK	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF

* RS880M can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.



INTERNAL CLOCK MODE



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Notebook R&D Division
Title: CLOCK DISTRIBUTION
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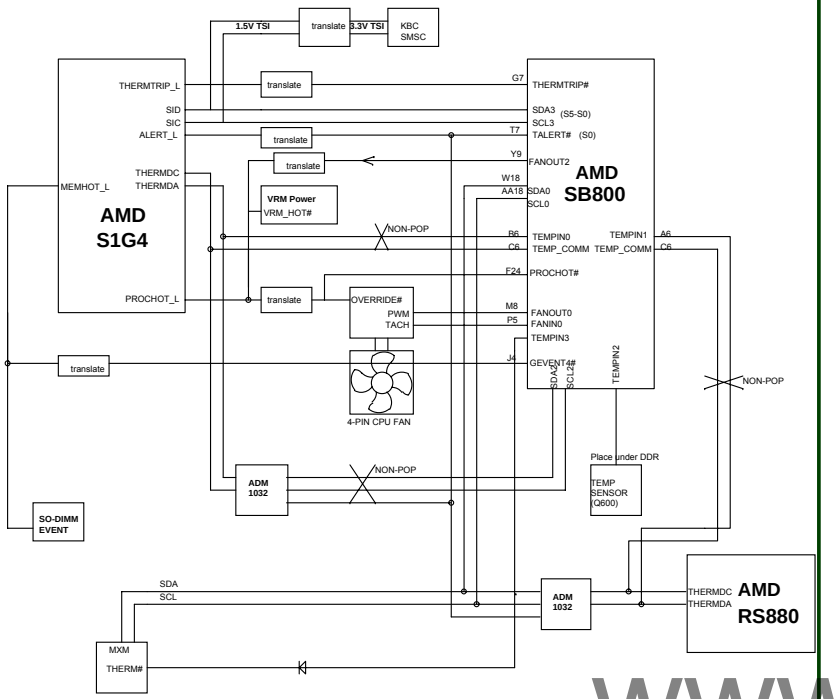
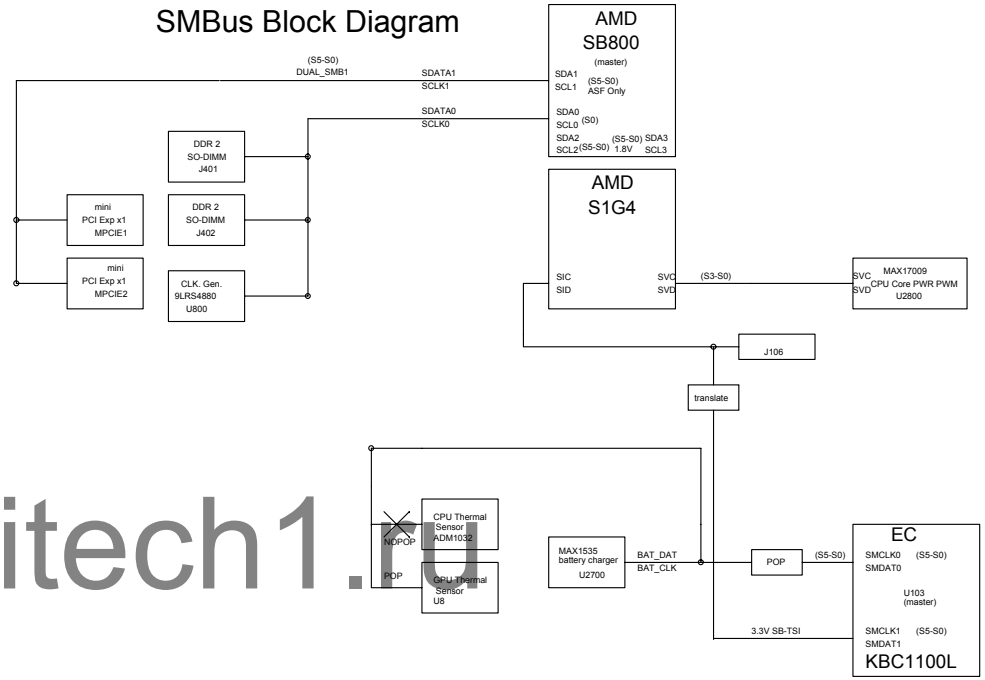
Thermal Systems
(Emergency Shutdown, Throttling, Fan Control)



Thermal disaster prevention is implemented by PROCHOT_L and THERMTRIP_L with hardware non-system dependant functions. Fan speed control will only be implemented by SB TSI software based implementation

SMBus Block Diagram



Power State / Voltage Rail Activity Summary

Global System State	Sleep State	Processor Power State	Description		RTC	ALW	DUAL	SUS	RUN
G0	S0	C0	Running		ON	ON	ON	ON	ON
G0	S0	C0	Running	P-state transitions under OS control	ON	ON	ON	ON	ON
G0	S0	C1		Halt	ON	ON	ON	ON	ON
G0	S0	C2		Stop grant, caches snoopable	ON	ON	ON	ON	ON
G0	S0	C3		TBD	ON	ON	ON	ON	ON
G0	S0	c4		TBD	ON	ON	ON	ON	ON
G1	S1	OFF	Sleeping	Powered on suspend	ON	ON	ON	ON	ON
G1	S3	OFF		Suspend to RAM	ON	ON	ON	ON	OFF
G2	S4	OFF		Suspend to diskON	ON	ON	ON	OFF	OFF
G2	S5	OFF	Soft-off		ON	ON	ON	OFF	OFF
G2/G3	S5 LOW	OFF	Battery IN		ON	ON	OFF	OFF	OFF
G3		OFF	Mechanical off		ON	OFF	OFF	OFF	OFF

Group Name Description

INT: Stuff when use internal clock generator
EXT: Stuff when use external clock generator
DNI/NC: DO NOT INSTALL
KBC: Stuff when use external KBC
IMC: Stuff when use internal EC
A11:Resistors marked with "A11" is only for SB800A11 ONLY.

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Title: MISCELLANEOUS TABLES

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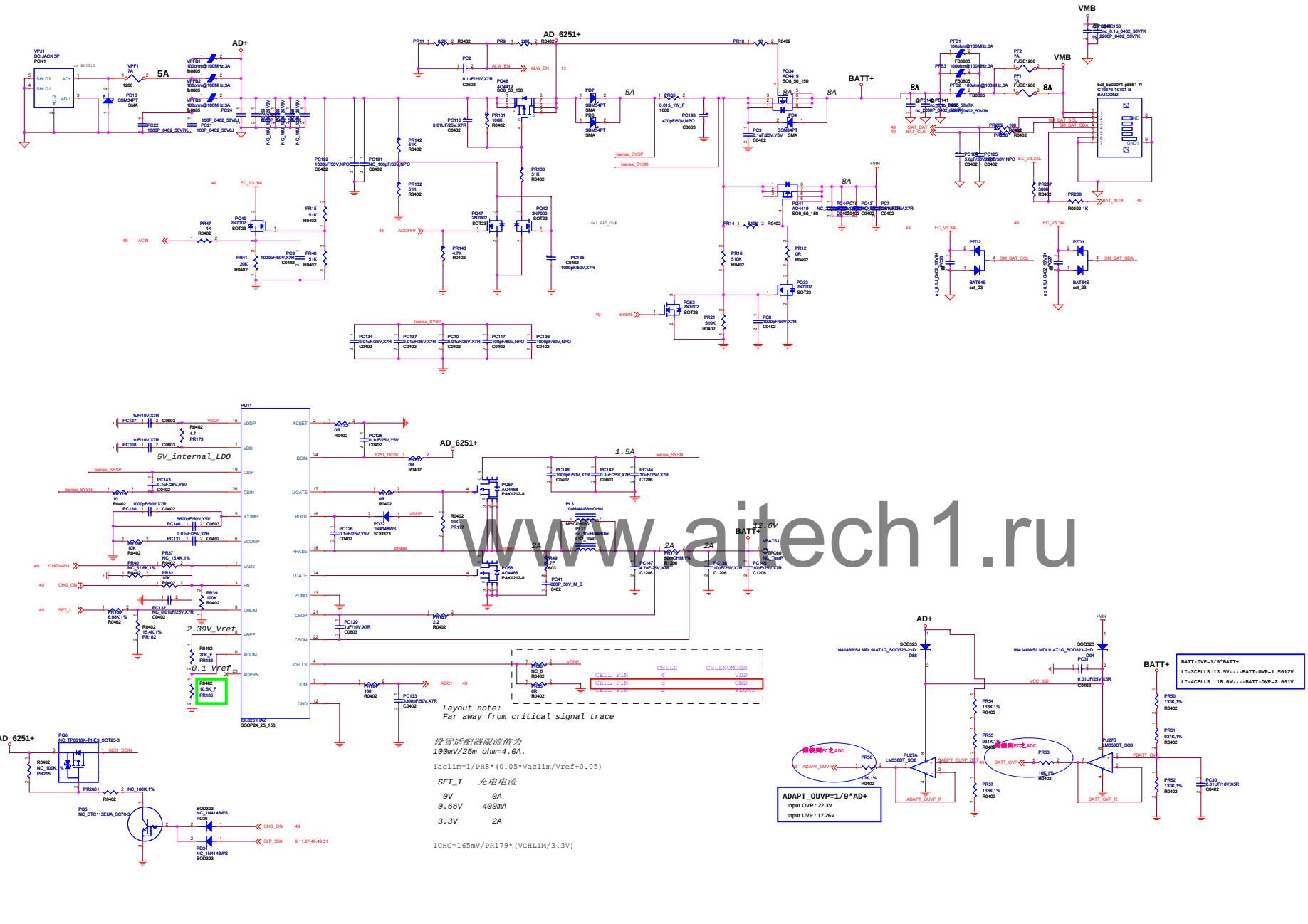

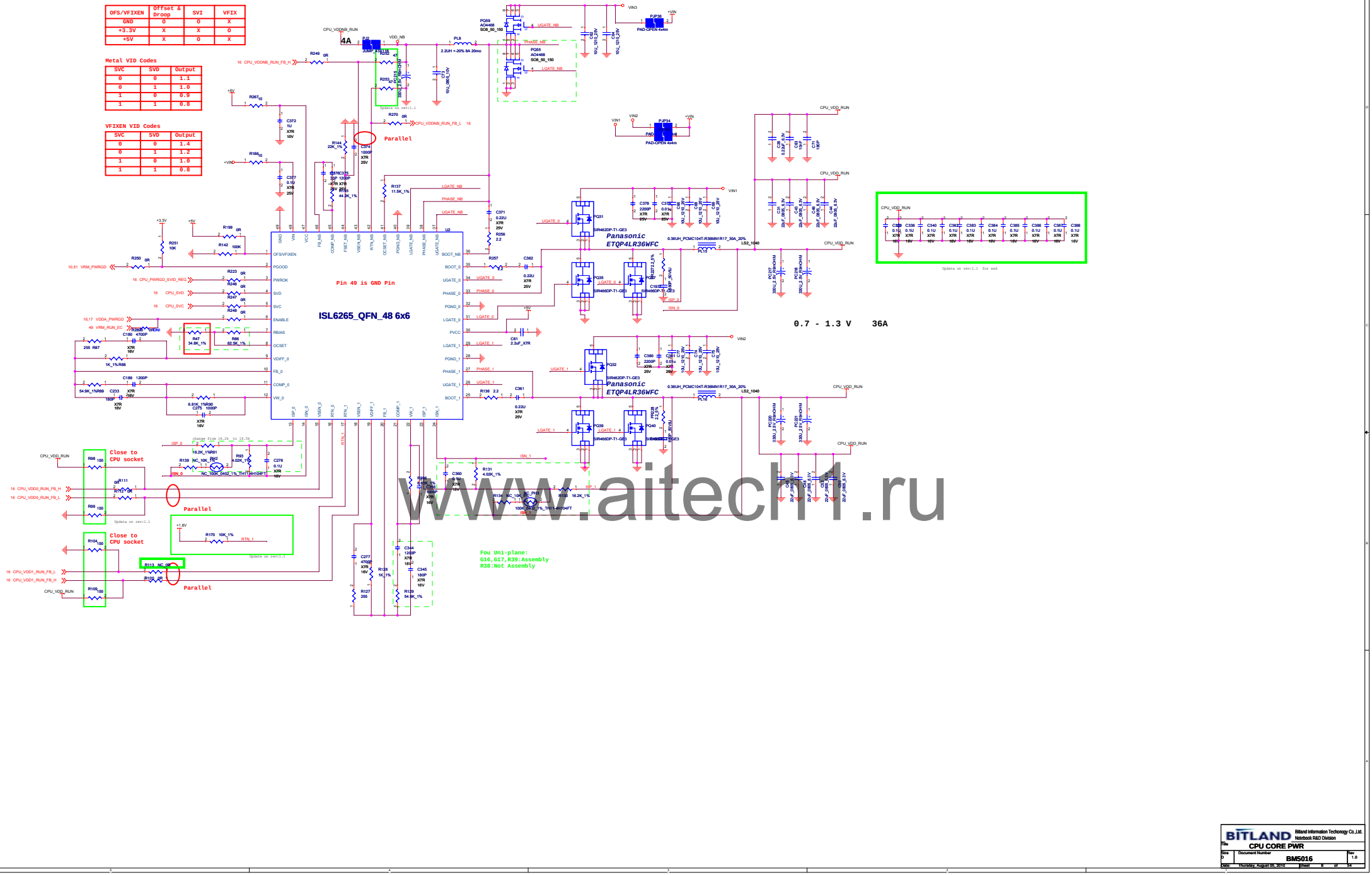

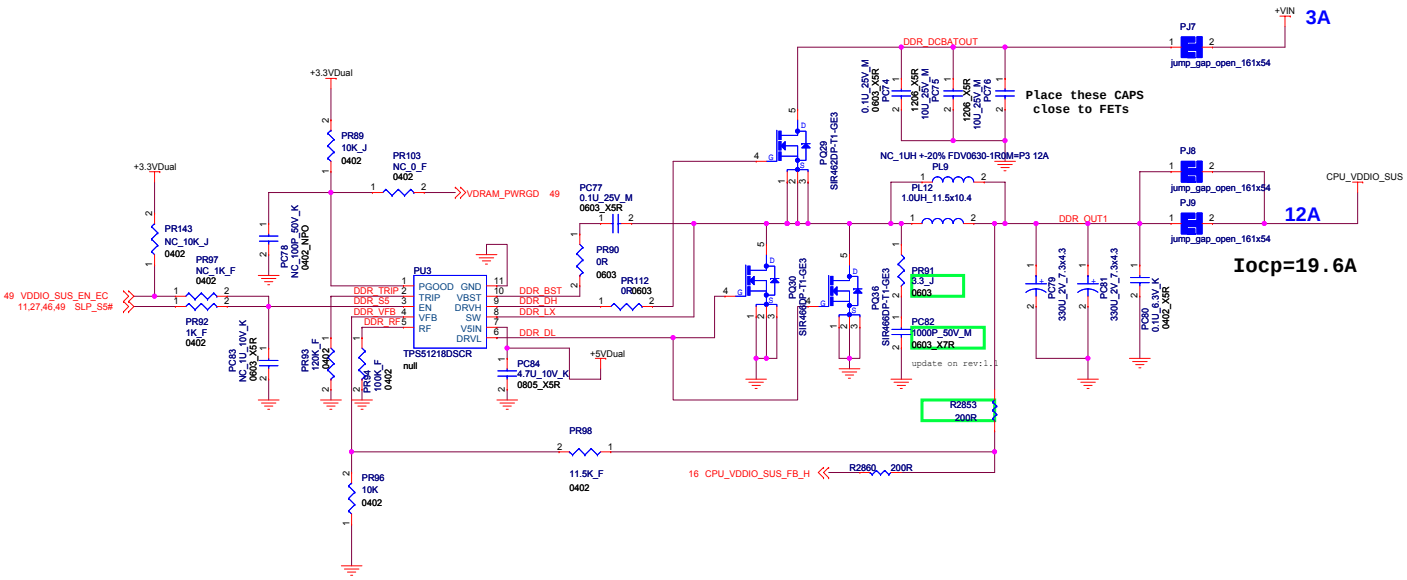

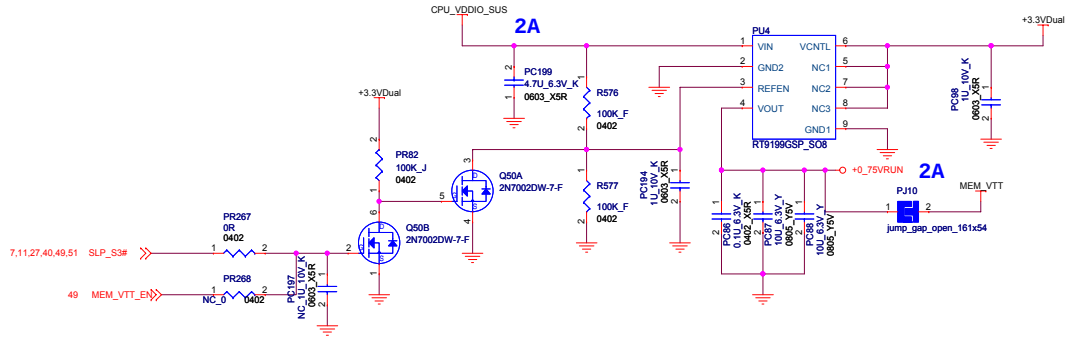

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Title: CPU MEM PWR

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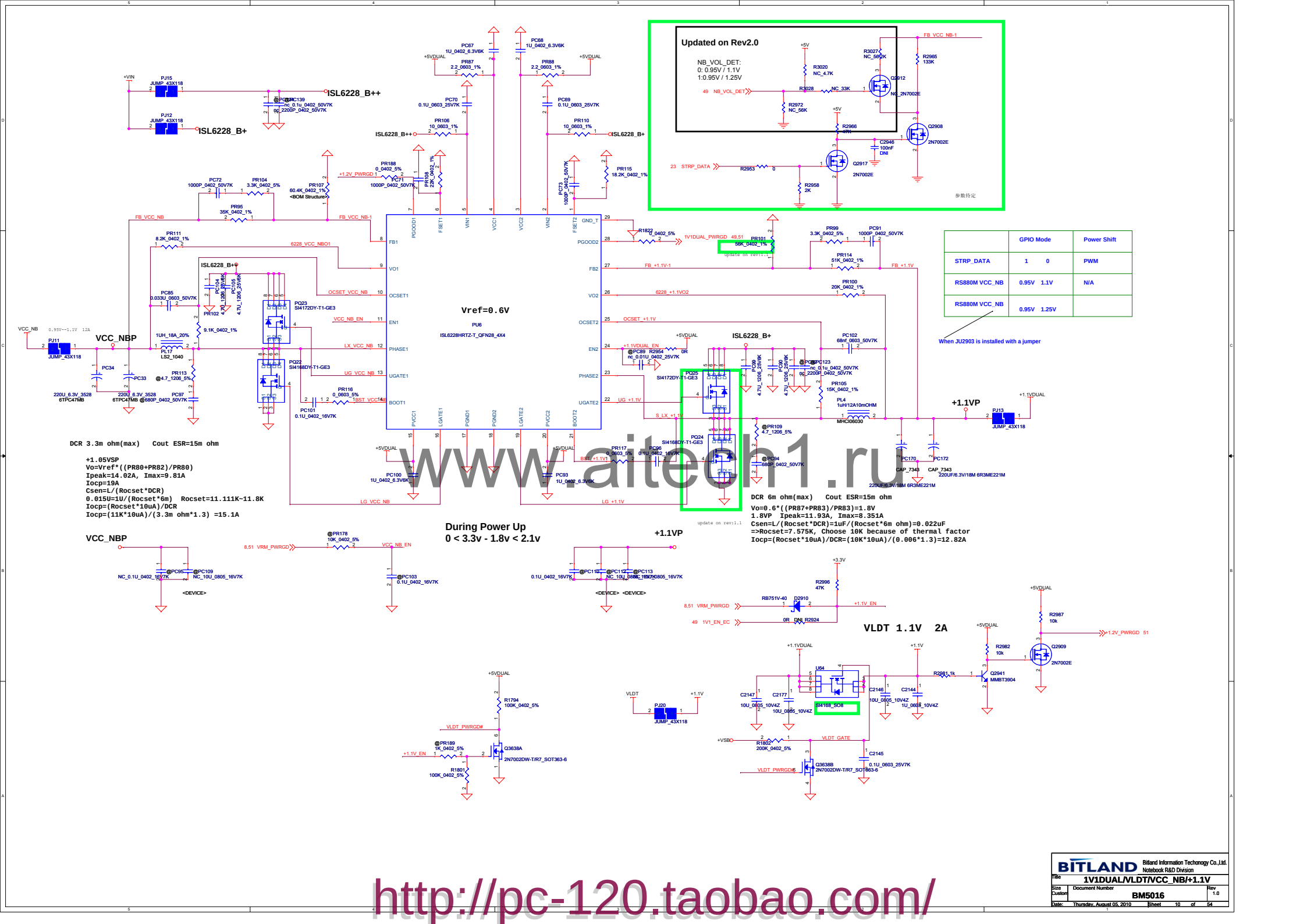
Updated on Rev2.0
NB_VOL_DET:
0: 0.95V / 1.1V
1:0.95V / 1.25V
Vref=0.6V
PU6
ISL6228HRTZ-T_QFN28_4X4
VCC_NBP
+1.1VP
+1.05VSP
Vo=Vref*((PR80+PR82)/PR80)
Ipeak=14.02A, Imax=9.81A
Iocp=19A
Csen=L/(Rocset*DCR)
0.015U=1U/(Rocset*6m) Rocset=11.111K~11.8K
Iocp=(Rocset*10uA)/DCR
Iocp=(11K*10uA)/(3.3m ohm*1.3) =15.1A
DCR 3.3m ohm(max) Cout ESR=15m ohm
DCR 6m ohm(max) Cout ESR=15m ohm
Vo=0.6*((PR87+PR83)/PR83)=1.8V
1.8VP Ipeak=11.93A, Imax=8.351A
Csen=L/(Rocset*DCR)=1uF/(Rocset*6m ohm)=0.022uF
=>Rocset=7.575K, Choose 10K because of thermal factor
Iocp=(Rocset*10uA)/DCR=(10K*10uA)/(0.006*1.3)=12.82A
During Power Up
0 < 3.3v - 1.8v < 2.1v
VLDT 1.1V 2A
When JU2903 is installed with a jumper
GPIO Mode
Power Shift
STRP_DATA
RS880M VCC_NB
0.95V 1.1V
PWM
N/A
1.25V
BITLAND
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Notebook R&D Division
1V1DUAL/VLDT/VCC_NB/+1.1V
BM5016
Thursday, August 05, 2010
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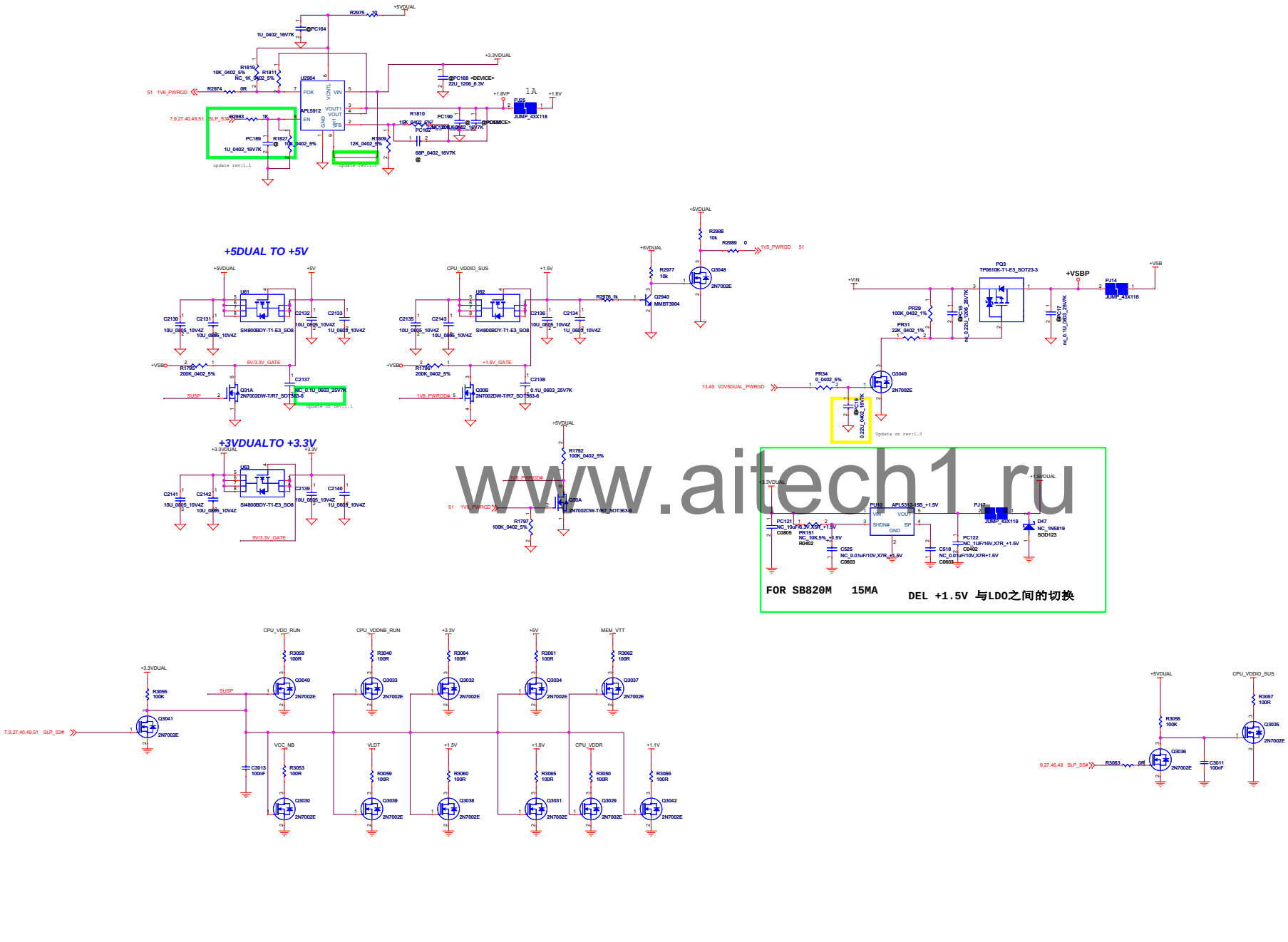
http://pc-120.taobao.com/



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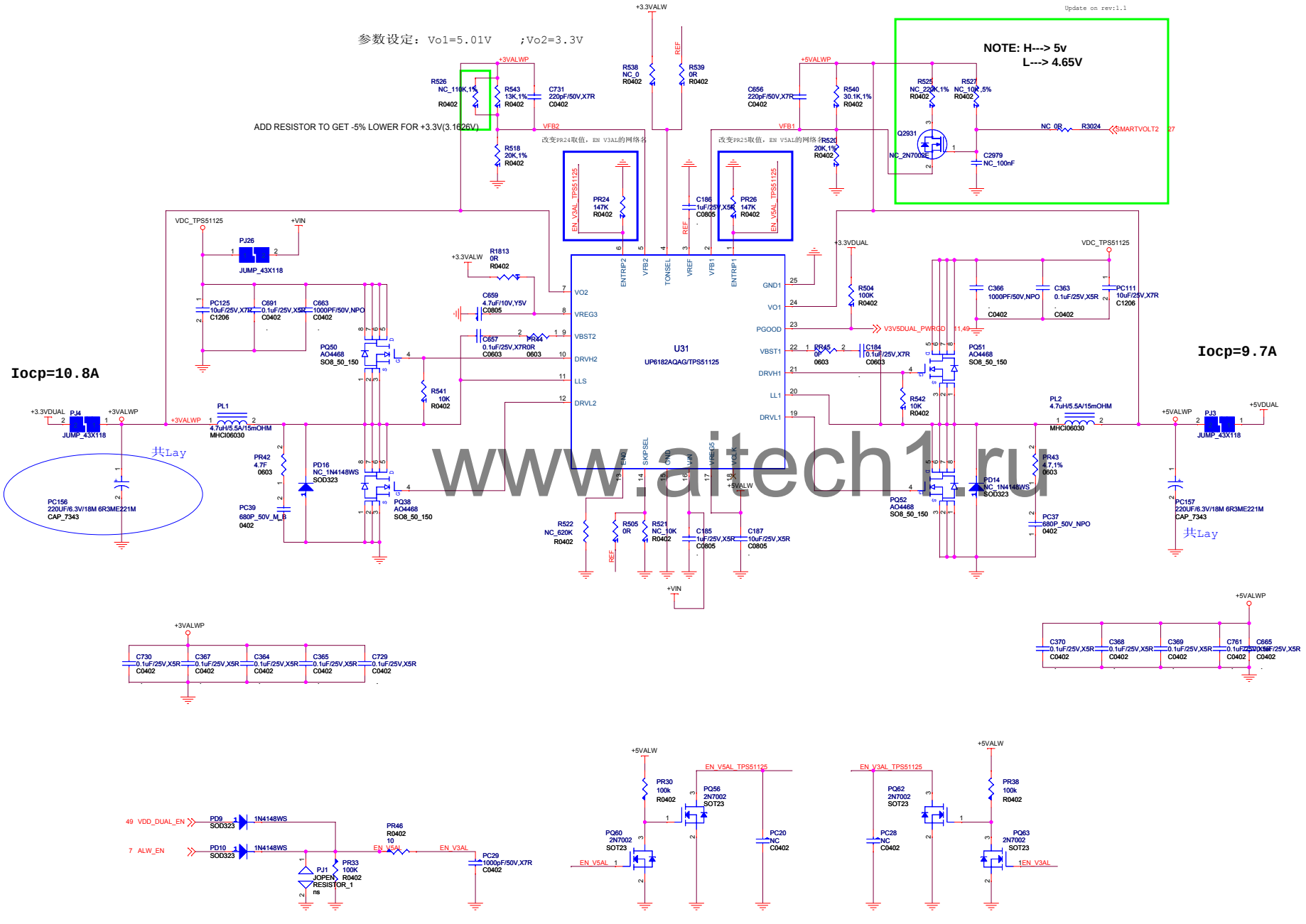

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Notebook R&D Division

Title: SYSTEM PWR

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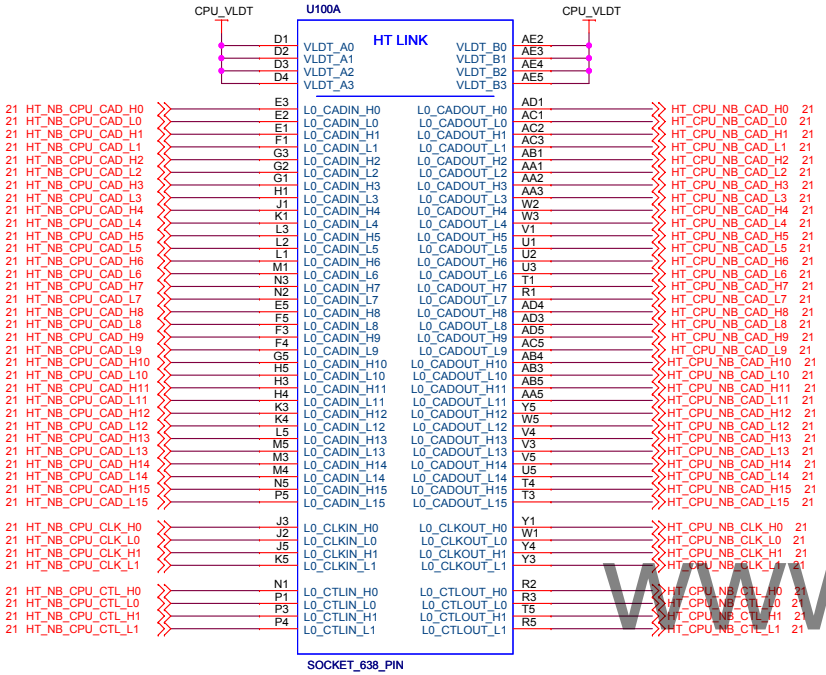
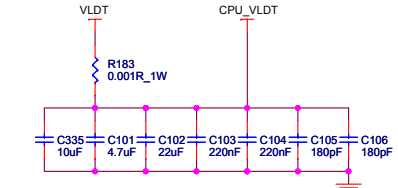
CPU_VLDT 1.1V 1.5A

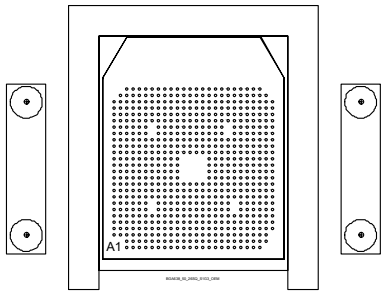


DEL HTPA Soft-Touch Duo Connectors



Place close to socket

* If VLDT is connected only on one side, one 4.7uF cap should be added to the island side



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	S1G4 HT I/F	
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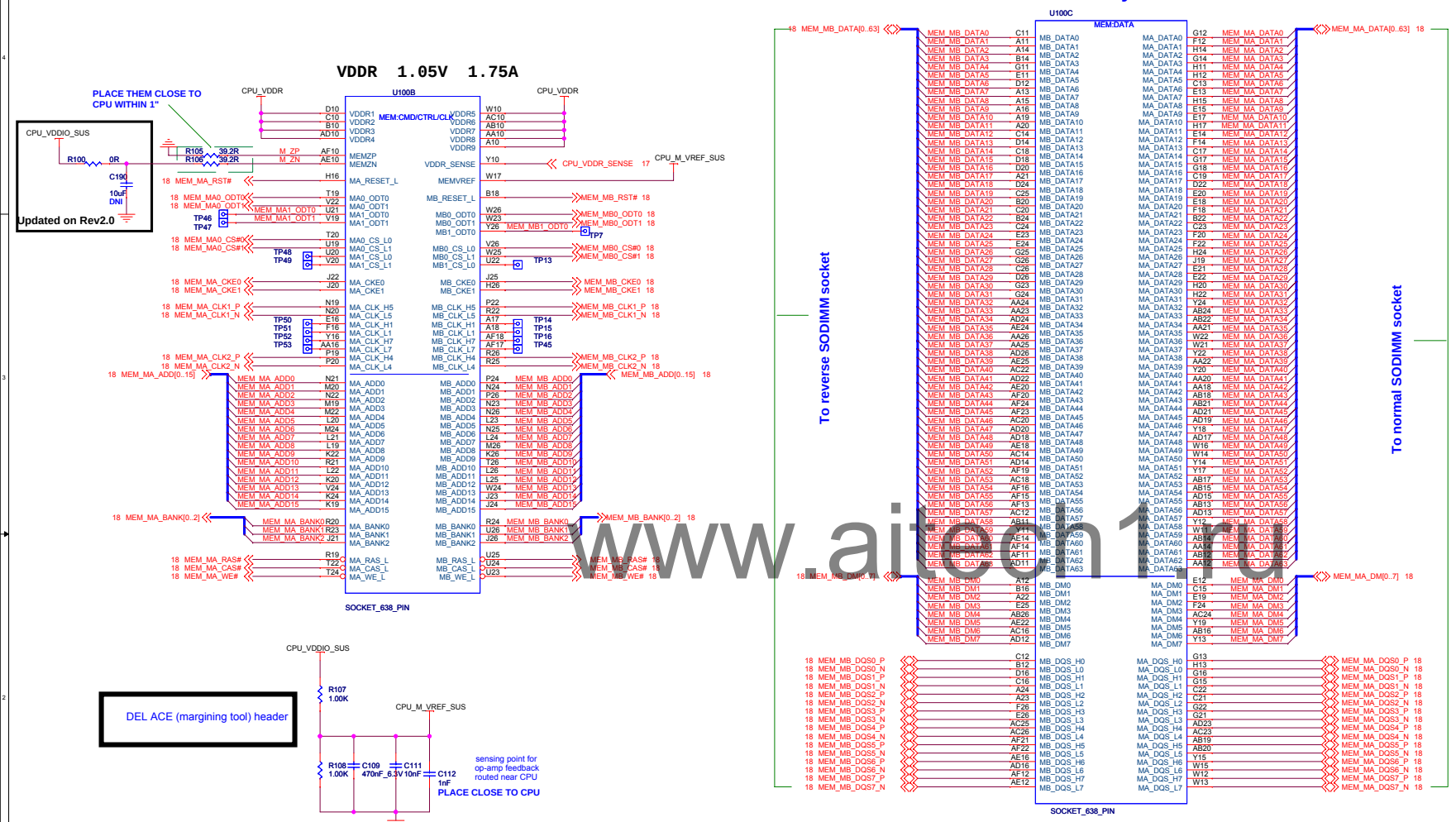
Processor Memory Interface



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division
Title	S1G4 DDRIII MEMORY I/F
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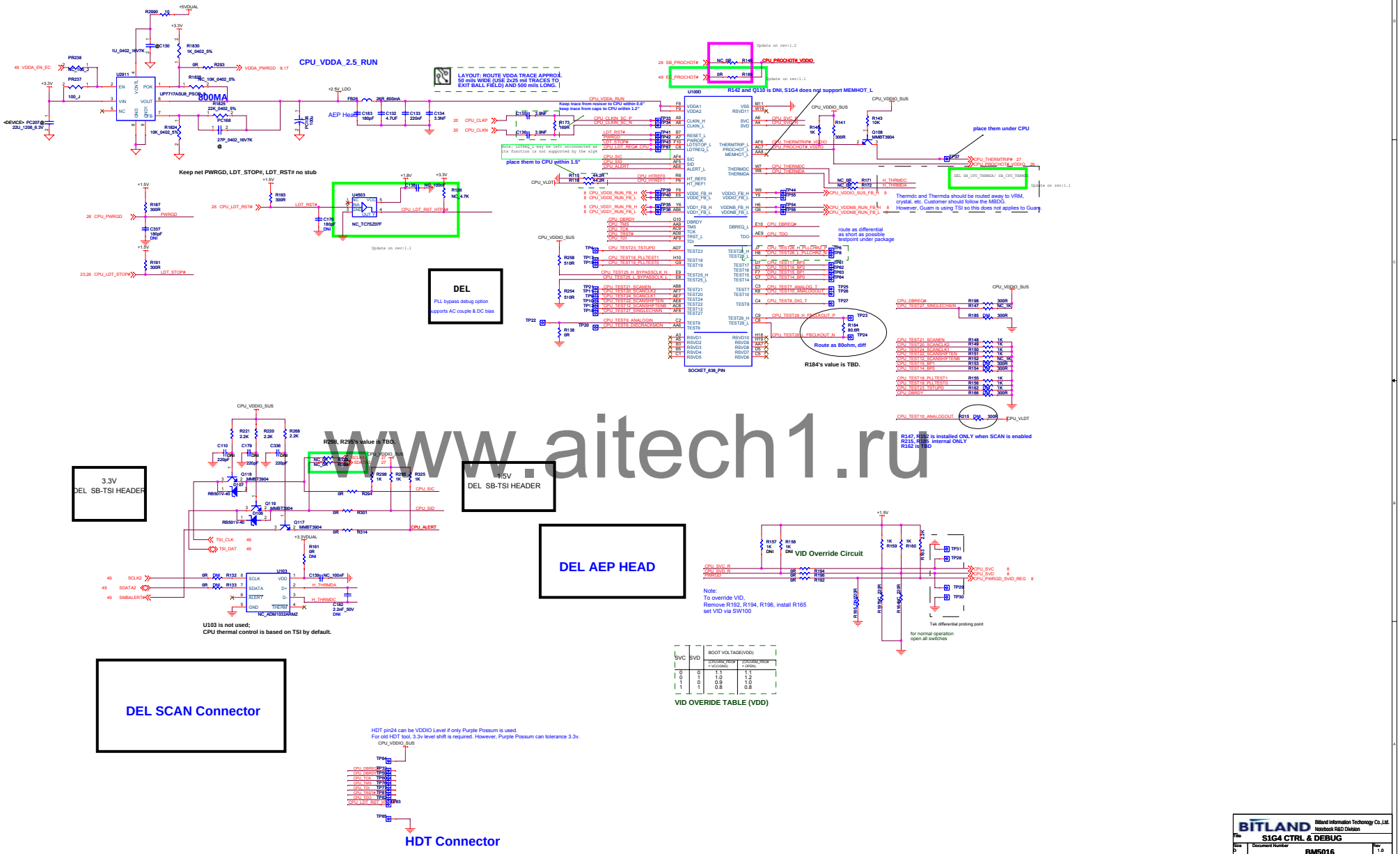

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Title: S1G4 CTRL & DEBUG

Size: D | Document Number: BM5016 | Rev: 1.0

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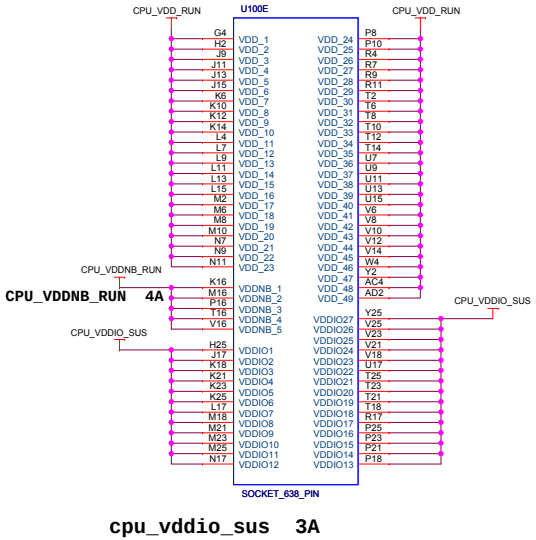
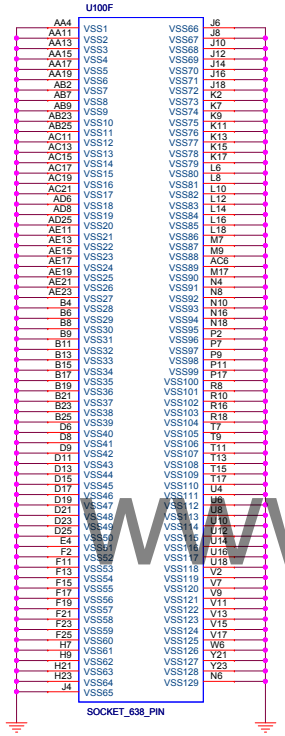
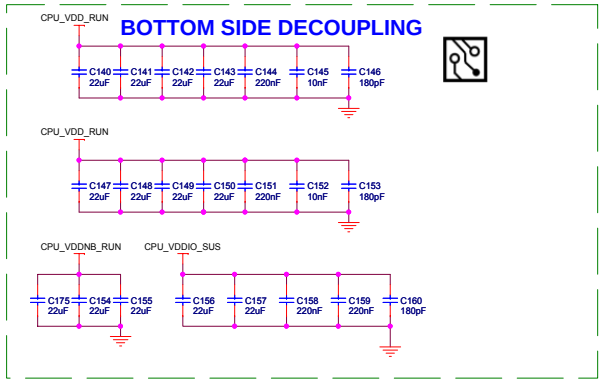
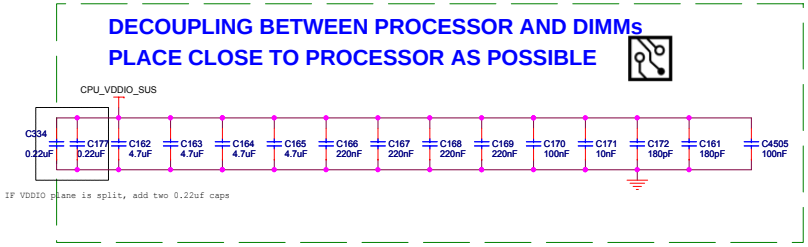
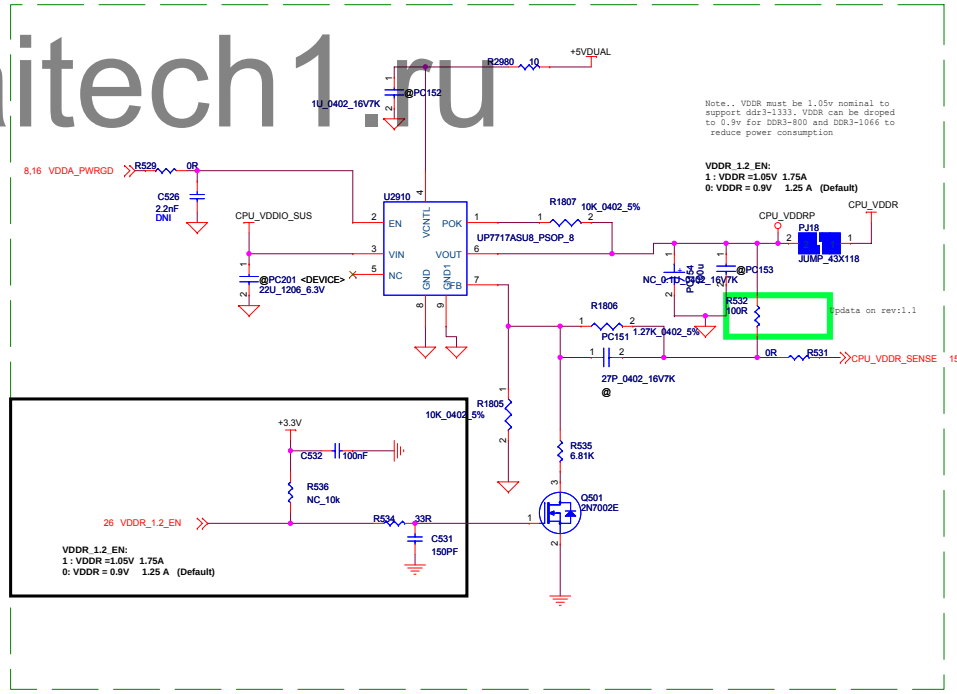


cpu_vddio_sus 3A









BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	S1G4 PWR & GND	
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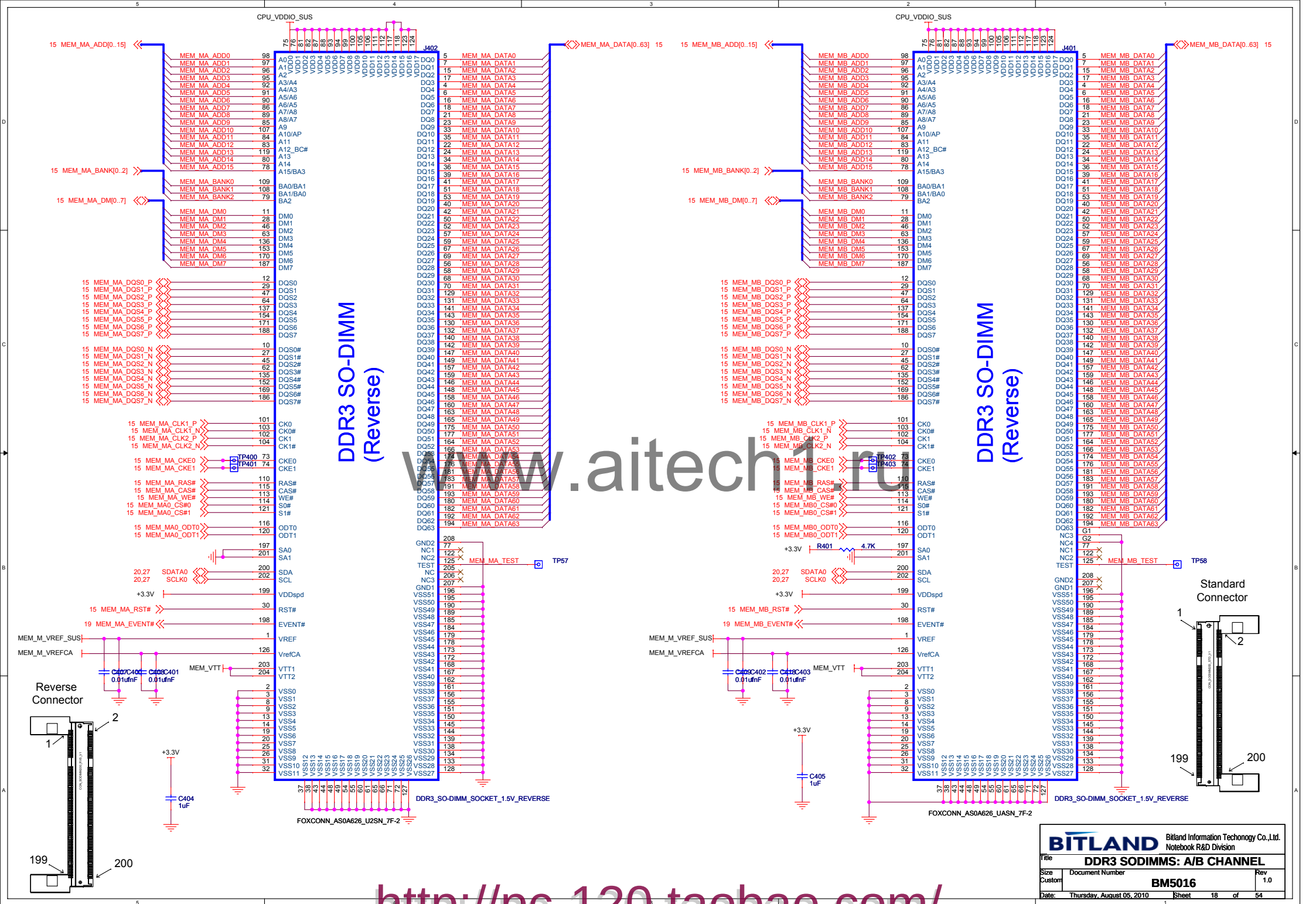
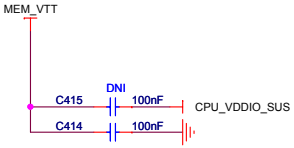
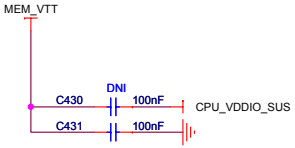
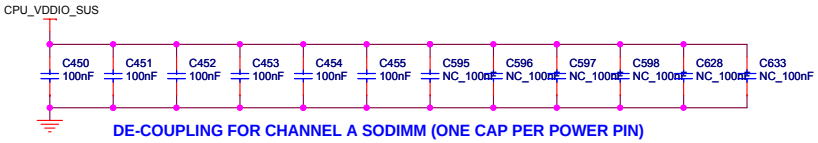




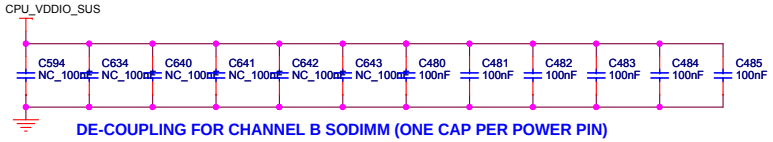
DE-COUPLING FOR CHANNEL A SODIMM



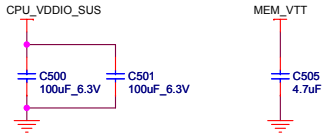
DE-COUPLING FOR CHANNEL B SODIMM

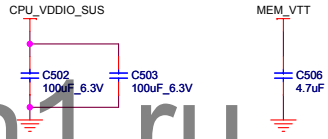


DE-COUPLING FOR CHANNEL A SODIMM (ONE CAP PER POWER PIN)

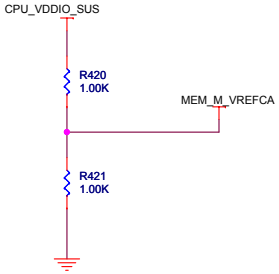


DE-COUPLING FOR CHANNEL B SODIMM (ONE CAP PER POWER PIN)

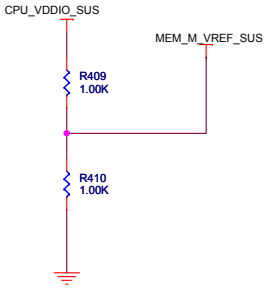




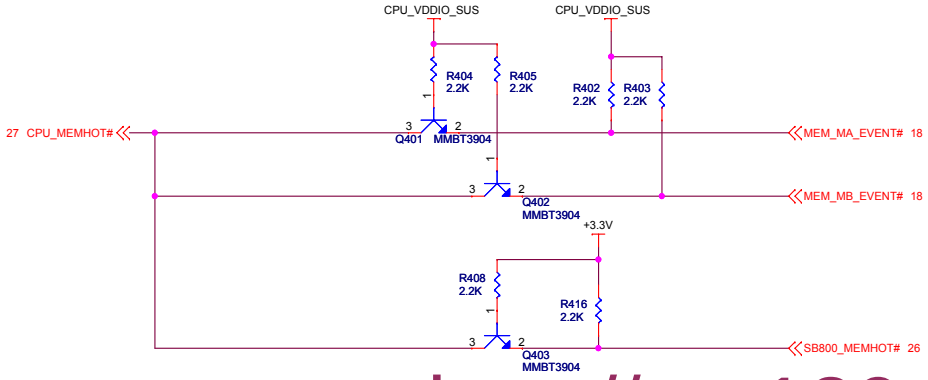
LAYOUT: PLACE CLOSE TO DIMMs



MEM_VREF_SUS



LAYOUT: PLACE CLOSE TO DIMMs



BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title: DDR3 SODIMM DECOUPLING

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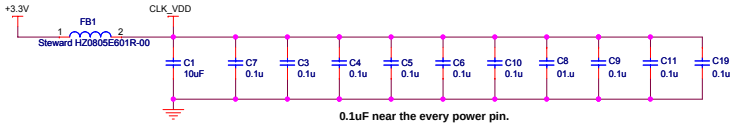
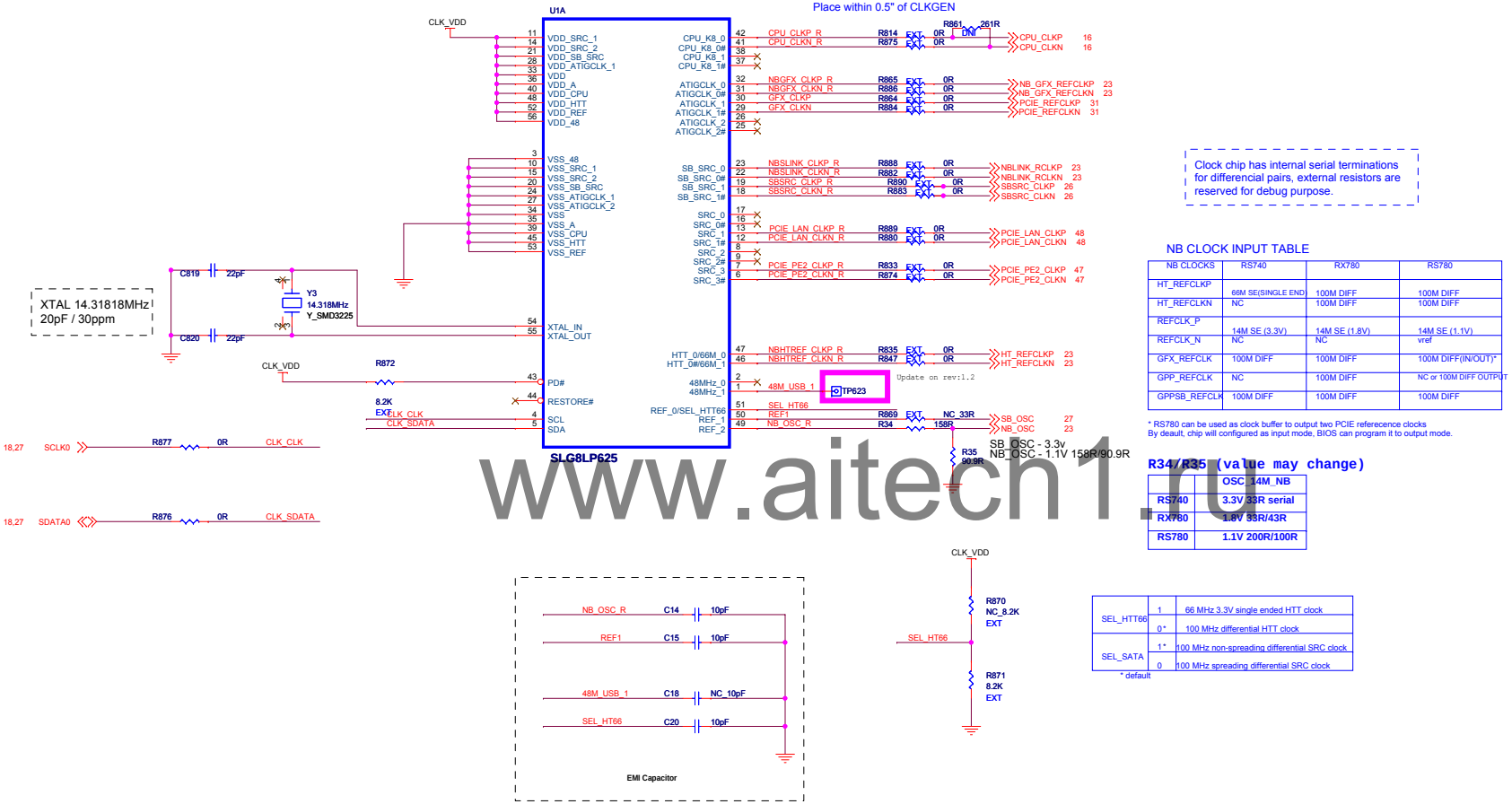


0.1uF near the every power pin.

Place within 0.5" of CLKGEN



Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

R34/R35 (value may change)

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 33R/43R
RS780	1.1V 200R/100R

SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock

* default

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Notebook R&D Division

Title: EXTERNAL CLOCK GENERATOR

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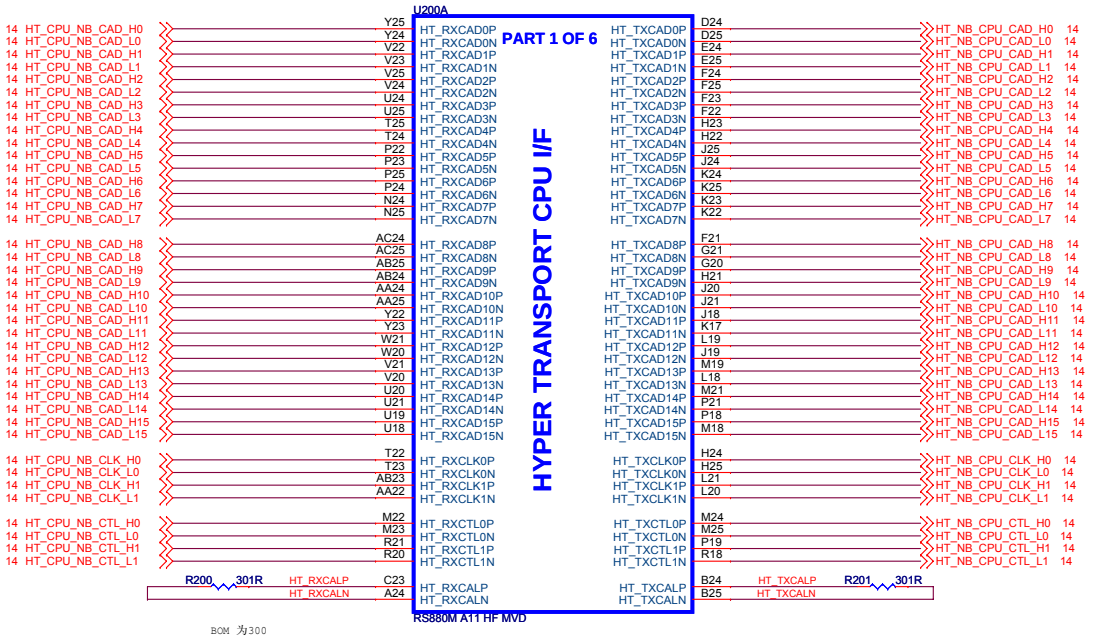

DEL HTPA PROBE CONNECTOR FOR DEBUG(NB SIDE)

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	RS880M-HT LINK I/F		
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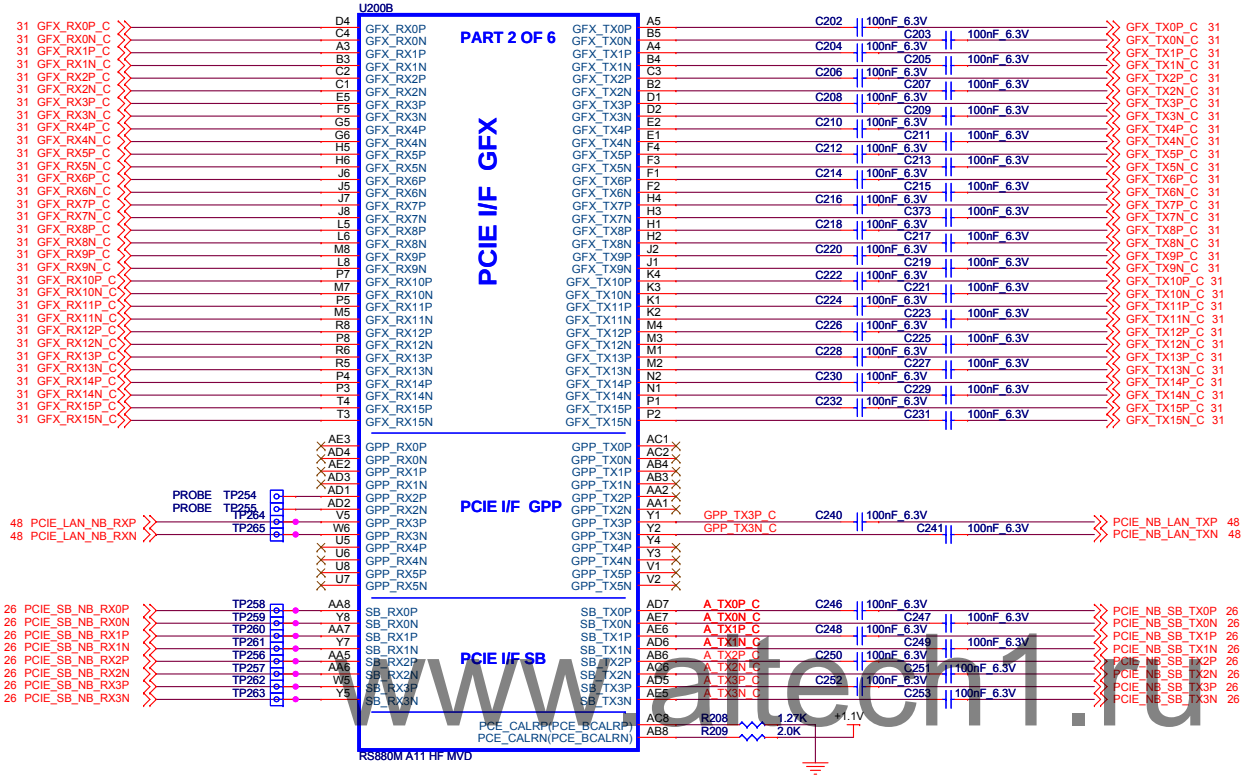
MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot

MXM3.0 need put the CAP on the motherboard.
Close to the MXM Slot



DEL header_1x3

Keep the impendance of PCIE lane to 85ohm +/-15%
Including the A-link

All PCIe lane shou route 8" max for Gen2 connector and max 12" for Gen2 on board devices
Guam has the Lasso lane over 8" due to the large board, should use shorter lasso calbe for Guam.
Customer need to follow the MBDG.

DEL PCIE MIDDLE BUS PROBE FOR DEBUG

RS880M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

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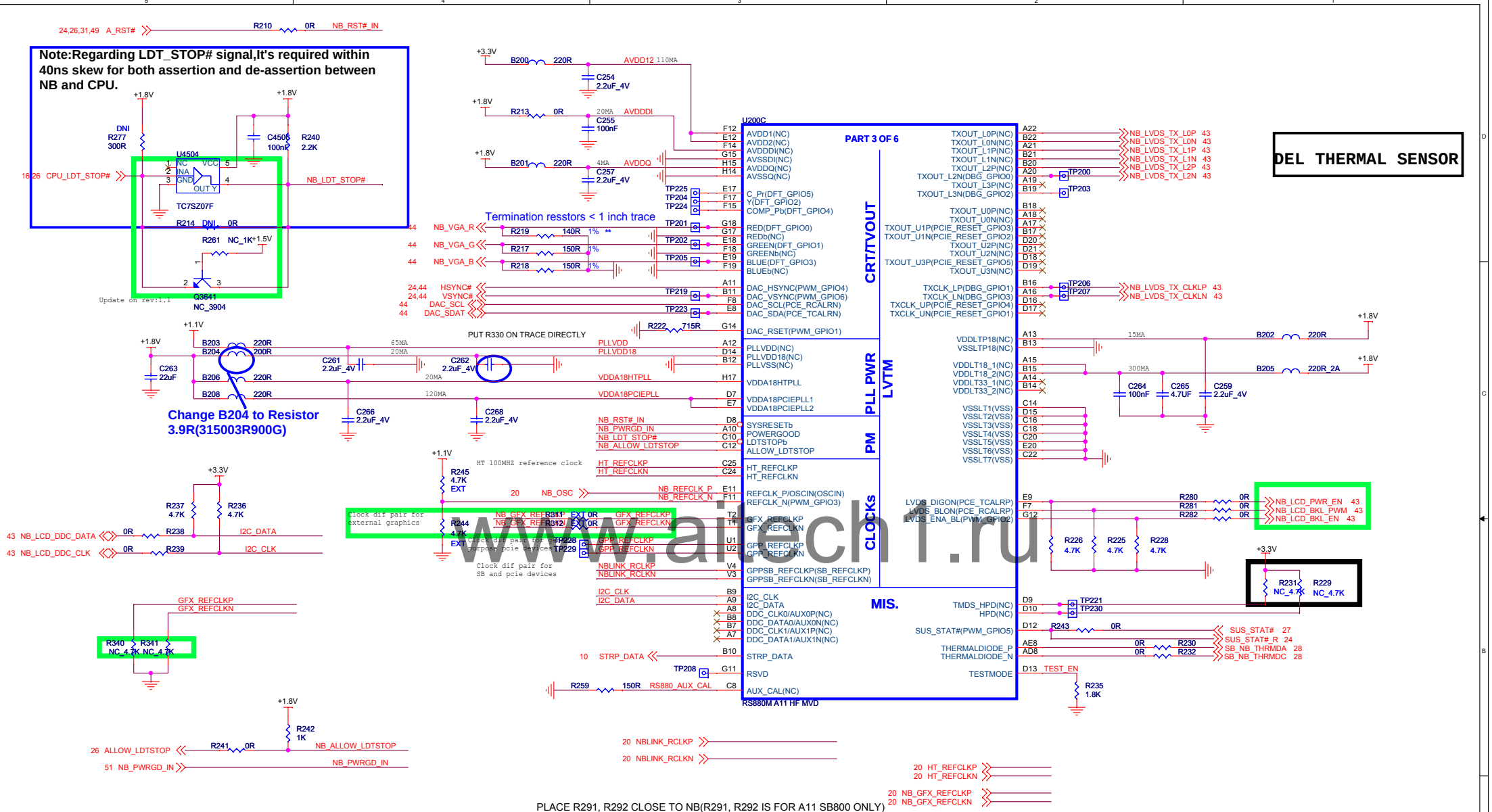
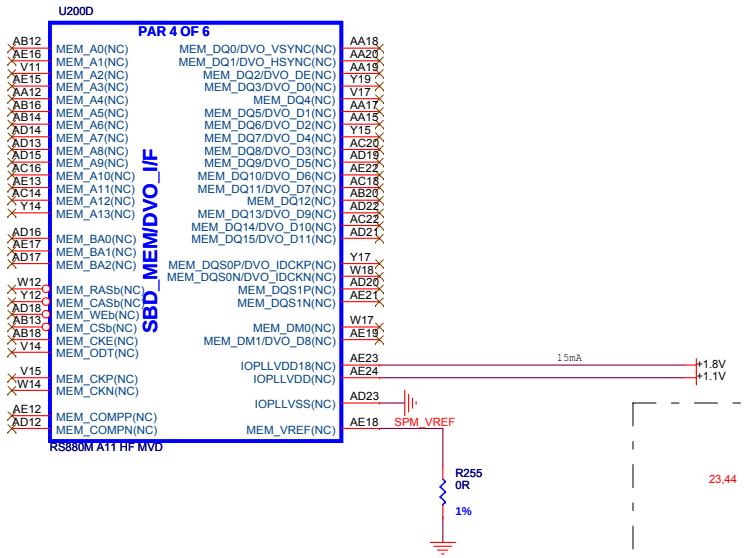
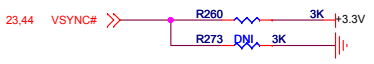
Title	RS880M-PCIE I/F	
Size / Custom	Document Number: BM5016	Rev: 1.0
Date: Thursday, August 05, 2010	Sheet 22 of 54	





DEL U202

DEL SDRAM DDR3

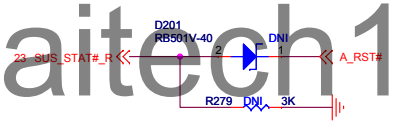


STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

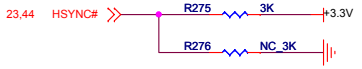
RS880M	
1 Disable	
0 Enable	

DFT_GPIO1: LOAD_EEPROM_STRAPS



Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected



RS880M: Enables Side port memory

RS880M:HSYNC#

Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

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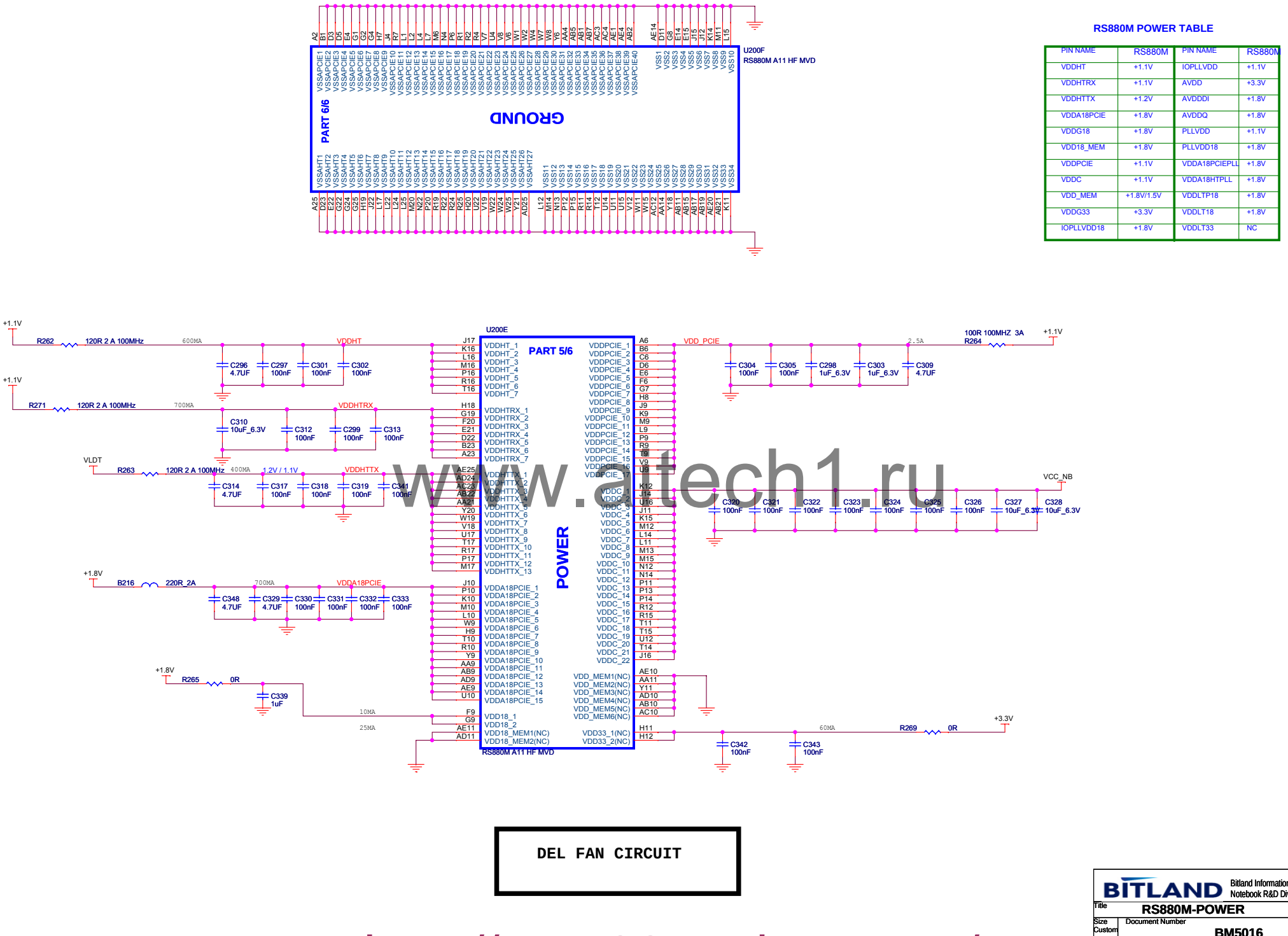
Title	RS880M-SPMEM/STRAPS	
Size: Custom	Document Number: BM5016	Rev: 1.0
Date: Thursday, August 05, 2010	Sheet 24 of 54	



RS880M POWER TABLE

PIN NAME	RS880M	PIN NAME	RS880M
VDDHT	+1.1V	IOPLLVDD	+1.1V
VDDHTRX	+1.1V	AVDD	+3.3V
VDDHTTX	+1.2V	AVDDDI	+1.8V
VDDA18PCIE	+1.8V	AVDDQ	+1.8V
VDDG18	+1.8V	PLLVDD	+1.1V
VDD18_MEM	+1.8V	PLLVDD18	+1.8V
VDDPCIE	+1.1V	VDDA18PCIEPLL	+1.8V
VDDC	+1.1V	VDDA18HTPLL	+1.8V
VDD_MEM	+1.8V/1.5V	VDDLTP18	+1.8V
VDDG33	+3.3V	VDDLT18	+1.8V
IOPLLVDD18	+1.8V	VDDLT33	NC

Bitland Information Techonogy Co.,Ltd.	Notebook R&D Division
Title	RS880M-POWER
Size / Custom	Document Number: BM5016
Rev	1.0
Date:	Thursday, August 05, 2010
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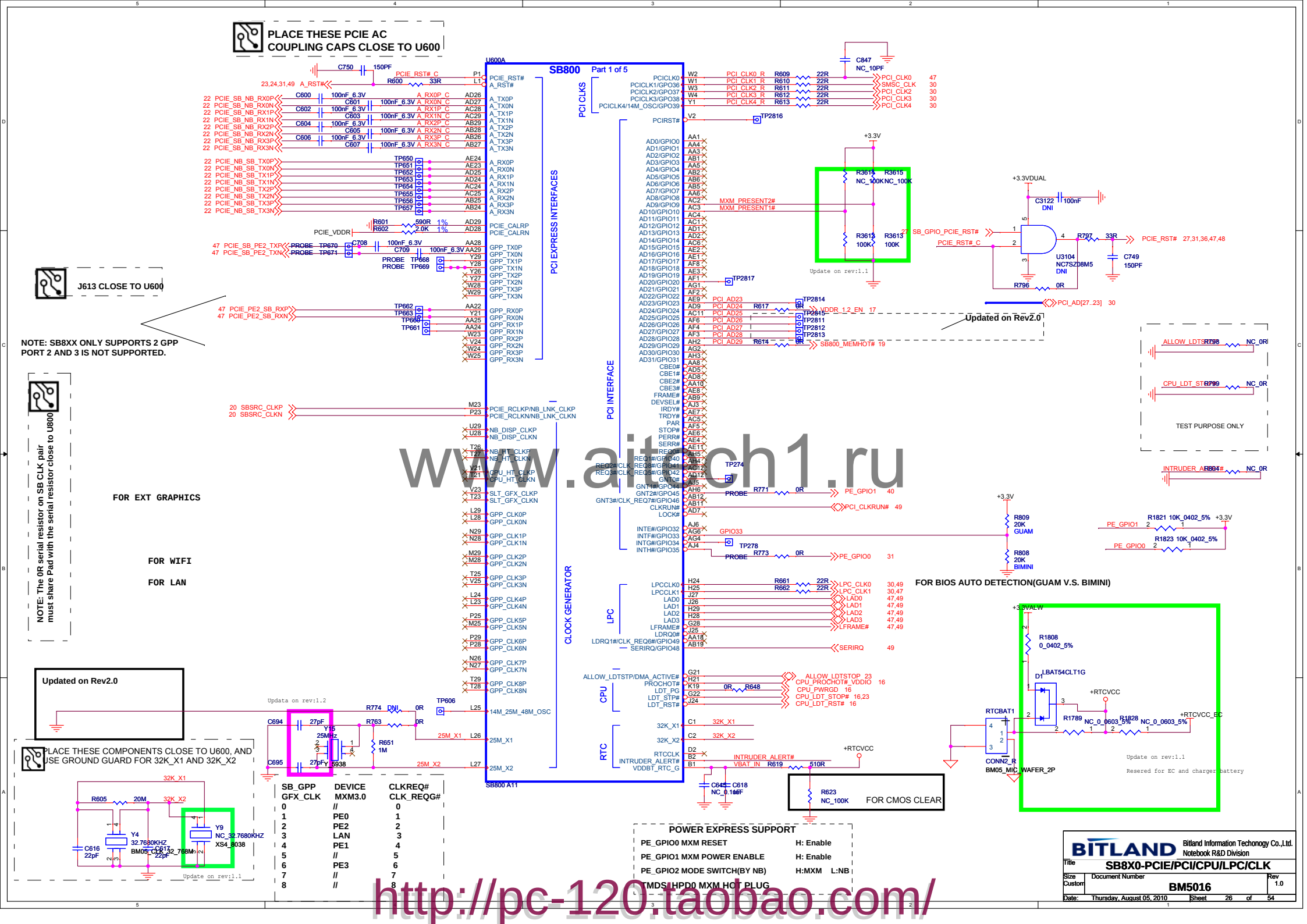
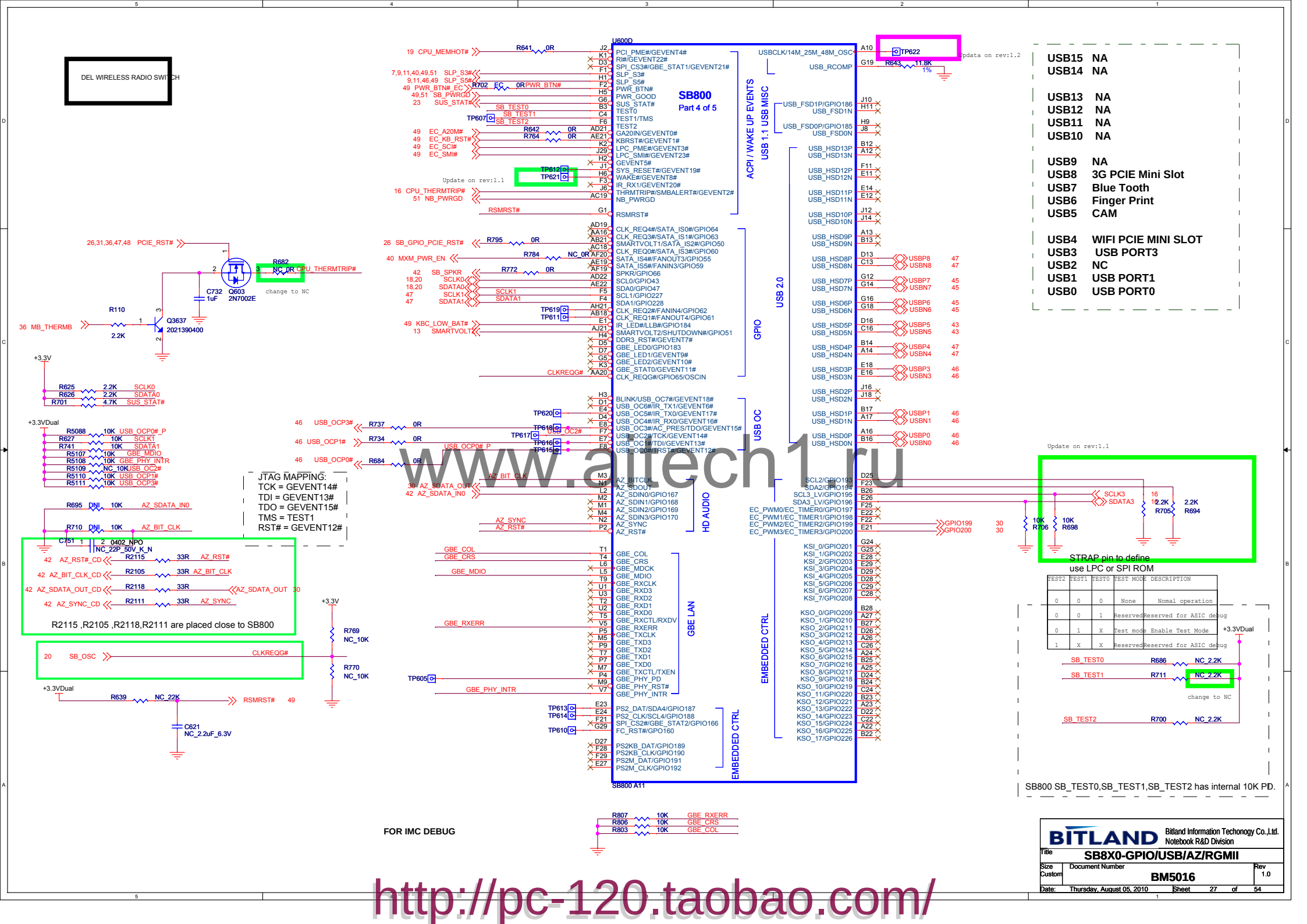




SATA trace should use only 1via on the trace. customers can use 2vias with GND via within 150mils of signal via as long as they can ensure that their platform meets SATA logo requirements. Return loss is expected to get affected with 2 vias. AMD platforms are validated with one via only

FOR SATA HD

FOR SATA ODD

SATA PORTS DISTRIBUTION:
0, - 2.5 INCH DISK DRIVER
1, SATA ODD
2,NOT USED
3, NOT USED
4 & 5, NOT USED

PLACE SATA_CAL RES VERY CLOSE TO BALL OF U600

To meet SB800 SCL1.02: DNI SATA XTAL circuit's parts

U600B

SB800
Part 2 of 5

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

SB800 A11

Connect C7 and D8, then go to GND directly.

NOTE: ROUTE TEMP_COMM AS A 10MIL TRACE

R685: Normal

R666: EXT Programmer

SST SPI ROM

change to SPI mode

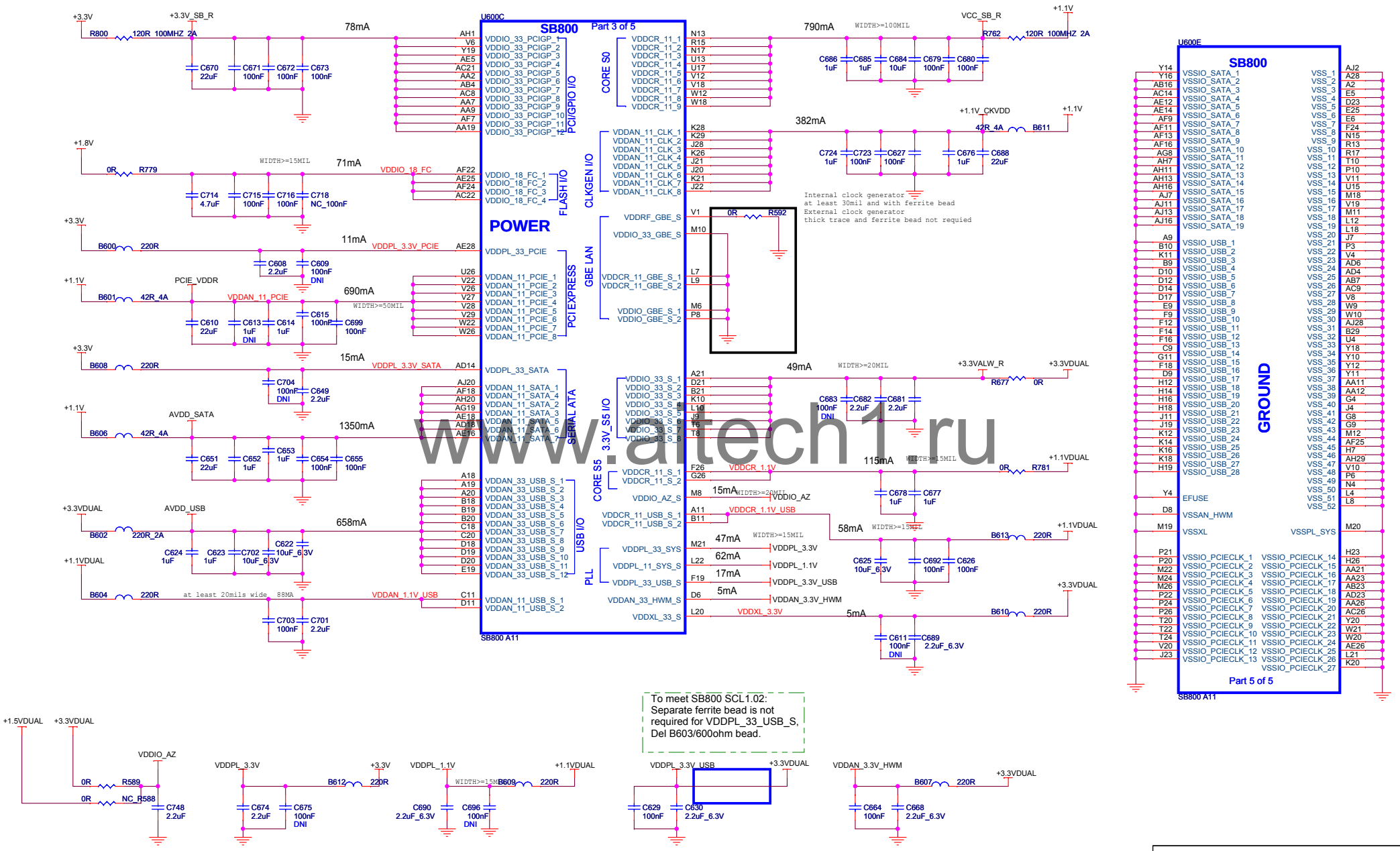
BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title: SB8X0-SATA/IDE/HWM/SPI

Size: Custom | Document Number: BM5016 | Rev: 1.0

Date: Thursday, August 05, 2010 | Sheet 28 of 54

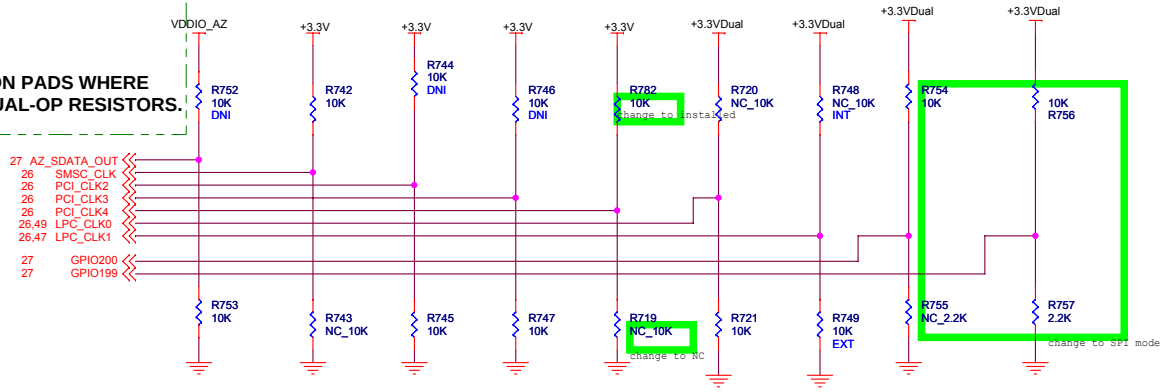
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



To meet SB800 SCL1.02:
Separate ferrite bead is not required for VDDPL_33_USB_S, Del B603/600ohm bead.

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division
Title	SB8X0-POWER & DECOUPLING
Size / Custom	Document Number: BM5016
Rev	1.0
Date:	Thursday, August 05, 2010
Sheet	29 of 54

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



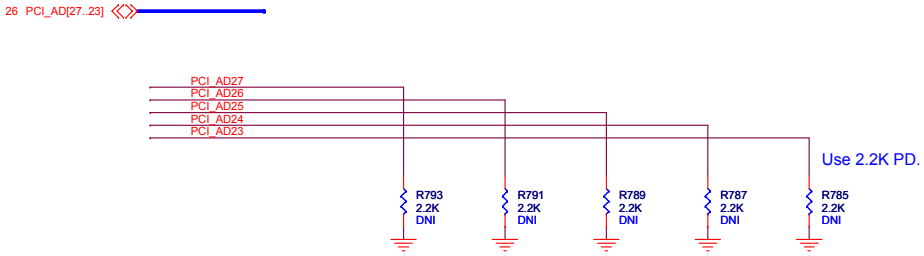
DEL JTAG HEADER

REQUIRED STRAPS

	AZ_SDOUT	SMSC_CLK	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM (Default) L,L = FWH ROM

DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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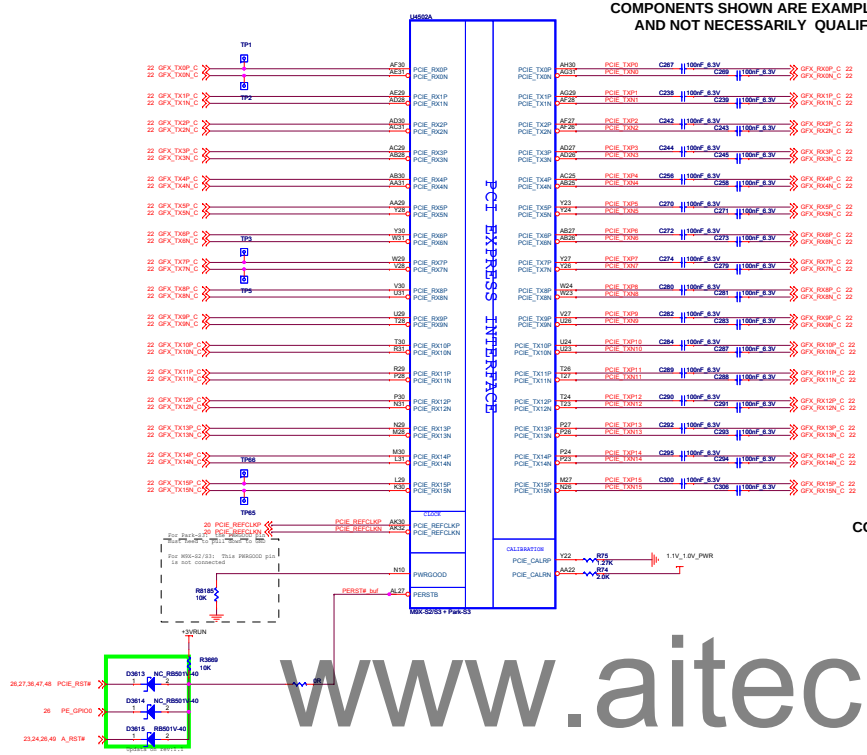
Title: SB8X0-STRAPS

Size: Custom | Document Number: BM5016 | Rev: 1.0

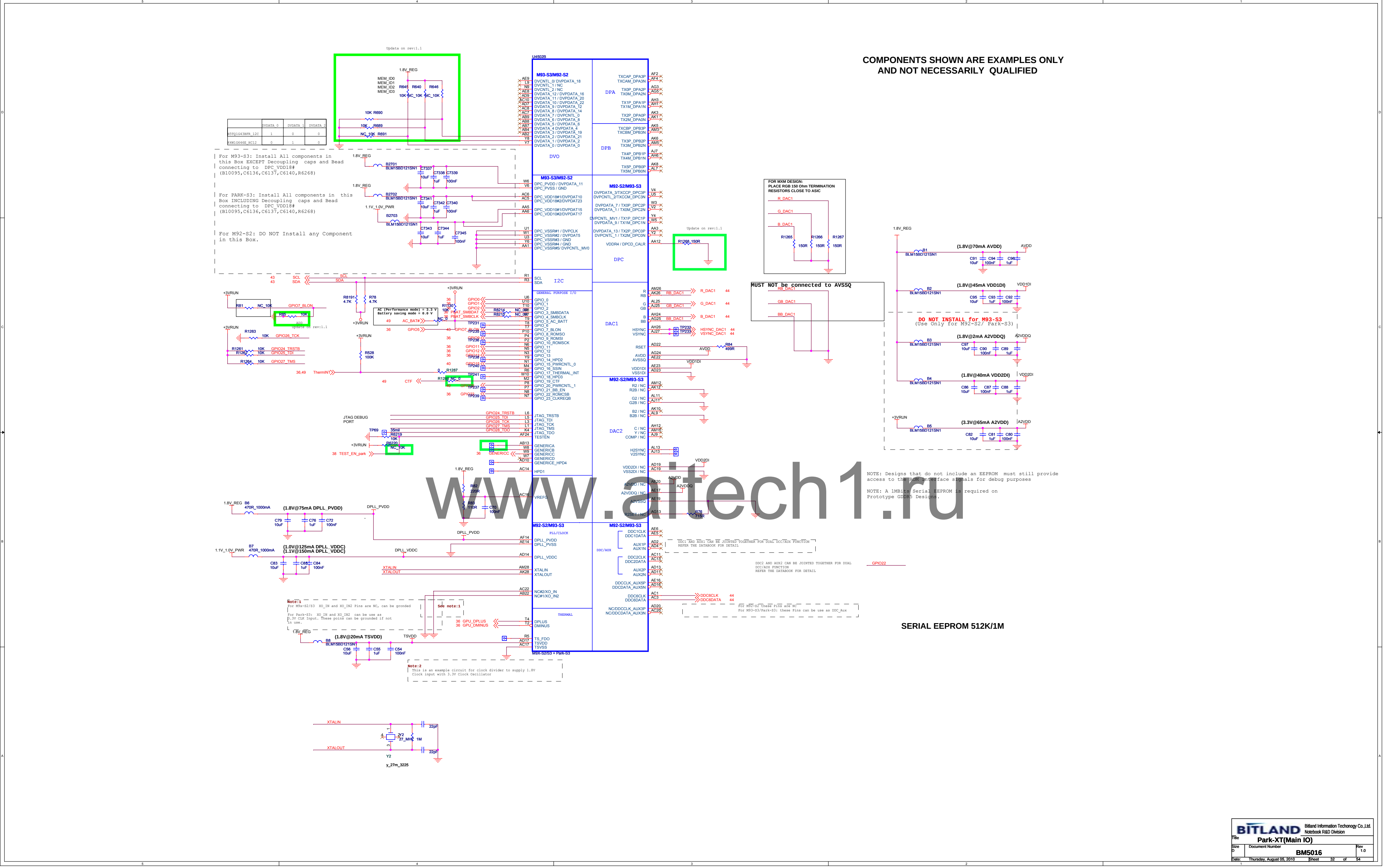
Date: Thursday, August 05, 2010 | Sheet 30 of 54

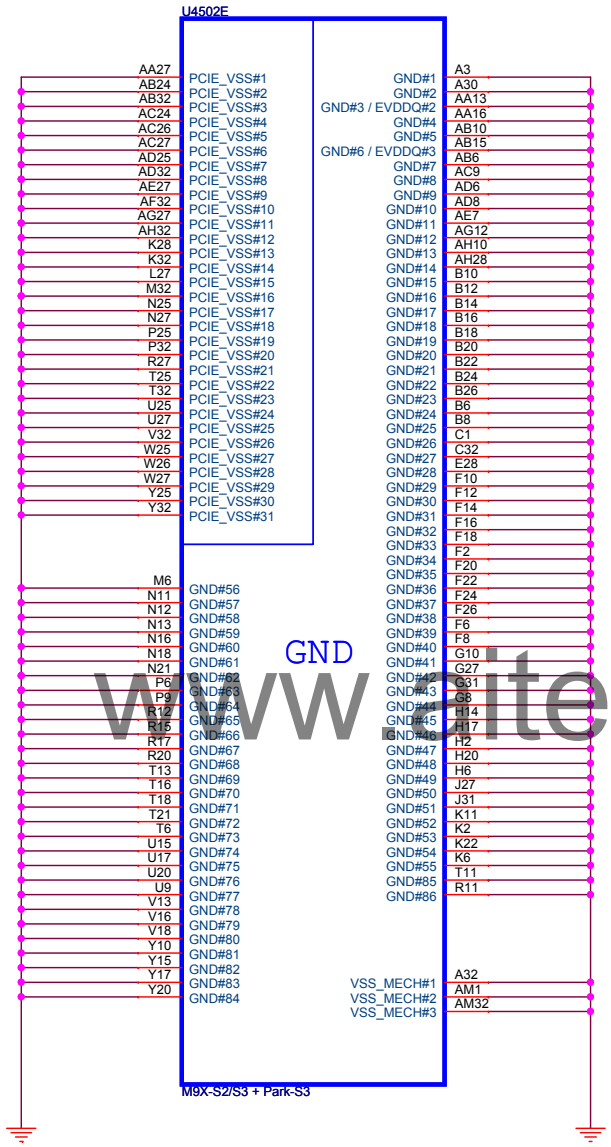
COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED



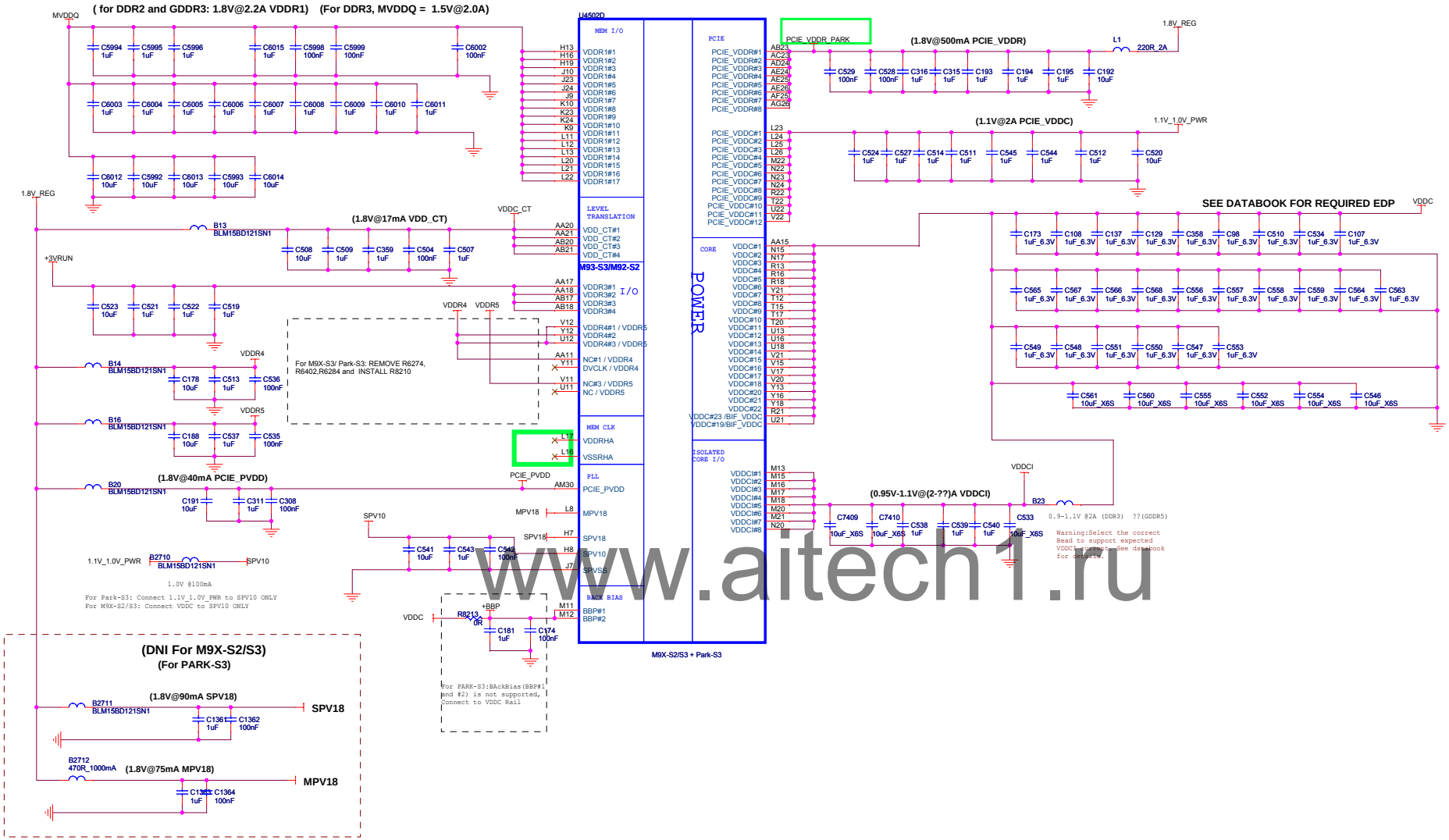
COMPONENTS SHOWN ARE EXAMPLES ONLY
AND NOT NECESSARILY QUALIFIED

BITLAND	Bitland Information Technology Co.,Ltd. Notebook R&D Division	
Title: Park-XT(PCI-E)		
Size: D	Document Number: BM5016	Rev: 1.0
Date: Thursday, August 05, 2010	Sheet 31 of 54	



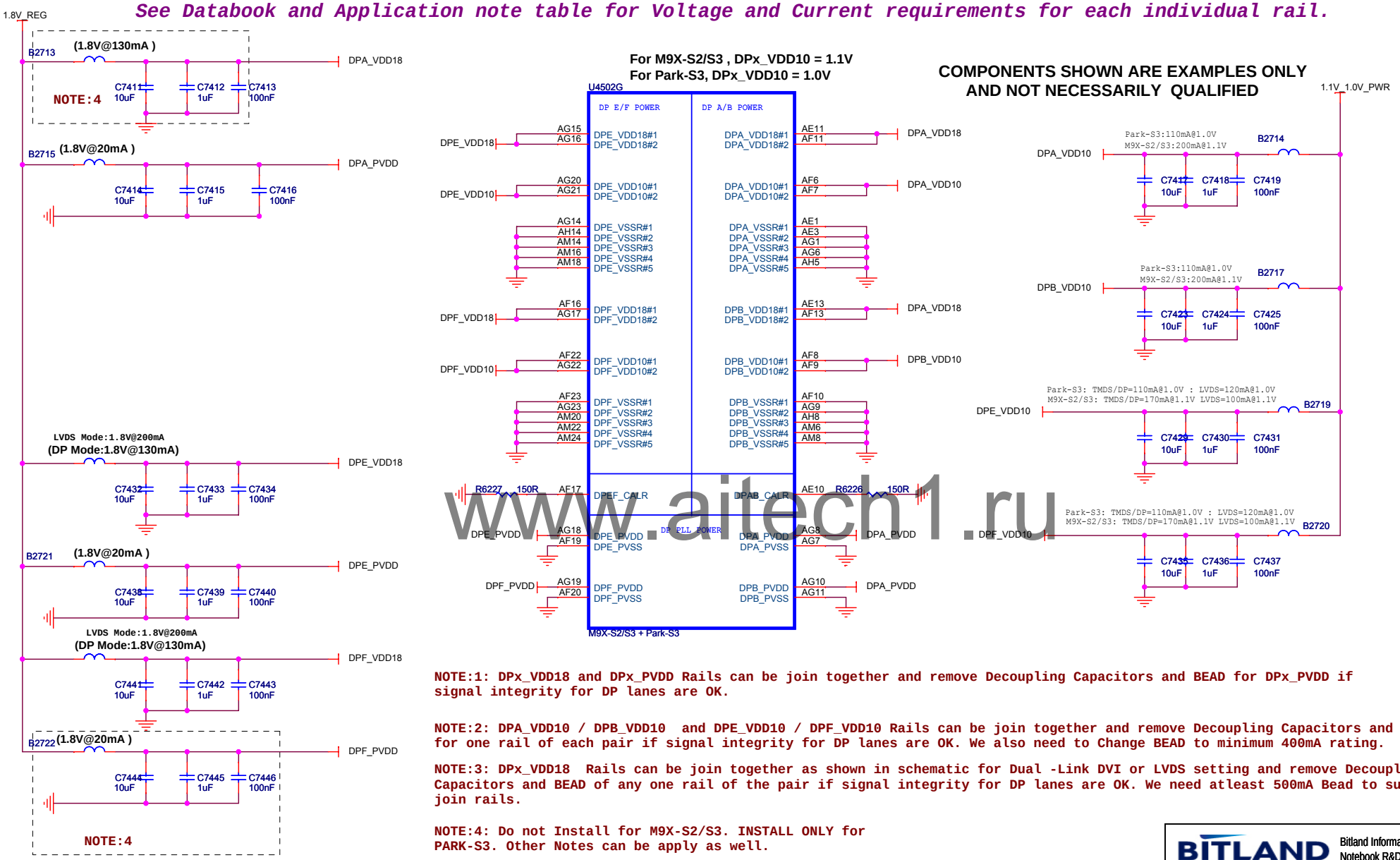


BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	PARK-XT(Core_GND)	
Size B	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 33 of 54	



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division		
Title	Park_XT(Power_and_NC)		
Size C	Document Number BM5016		Rev 1.0
Date: Thursday, August 05, 2010	Sheet 34 of 54		

See Databook and Application note table for Voltage and Current requirements for each individual rail.



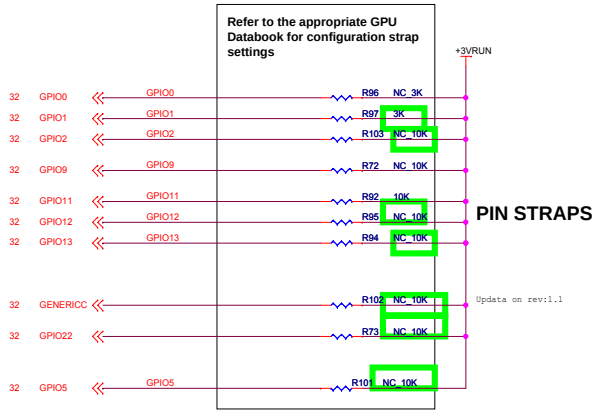
NOTE:1: DPx_VDD18 and DPx_PVDD Rails can be join together and remove Decoupling Capacitors and BEAD for DPx_PVDD if signal integrity for DP lanes are OK.

NOTE:2: DPA_VDD10 / DPB_VDD10 and DPE_VDD10 / DPF_VDD10 Rails can be join together and remove Decoupling Capacitors and BEAD for one rail of each pair if signal integrity for DP lanes are OK. We also need to Change BEAD to minimum 400mA rating.

NOTE:3: DPx_VDD18 Rails can be join together as shown in schematic for Dual -Link DVI or LVDS setting and remove Decoupling Capacitors and BEAD of any one rail of the pair if signal integrity for DP lanes are OK. We need atleast 500mA Bead to support join rails.

NOTE:4: Do not Install for M9X-S2/S3. INSTALL ONLY for PARK-S3. Other Notes can be apply as well.

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	Park-XT(DP Power)	
Size B	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 35 of 54	



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_GEN2_EN_A	GPIO2	PCIE GEN2 ENABLED	X
RSVD	GPIO8		0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	X
RSVD	GENERICC		0
AUD[1]	HSYNC	AUD[1] AUD[0]	0
AUD[0]	VSYNC	0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	X X

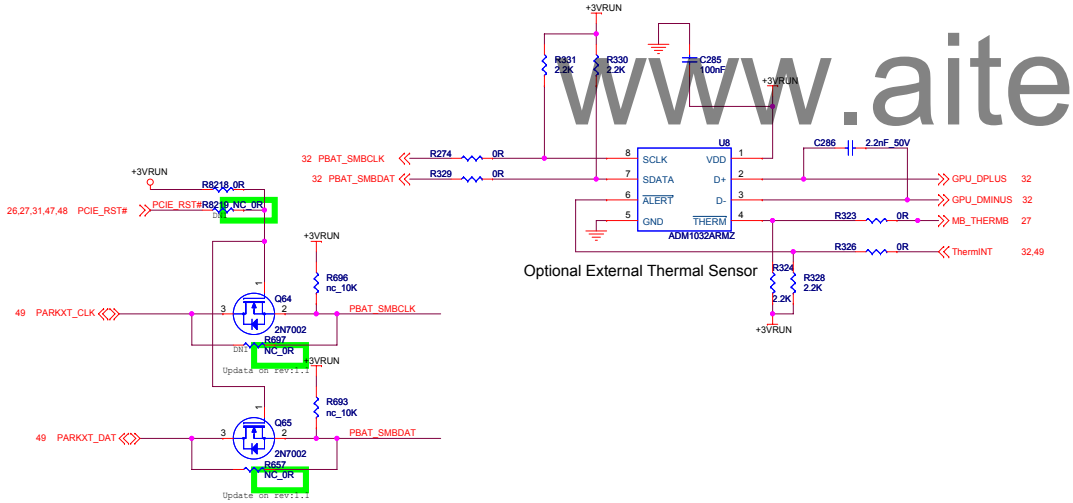
AMD RESERVED CONFIGURATION STRAPS

Provide pull-up pads for these straps - but do not populate. GPIOs functions on these signals must not conflict with the pin strap at Reset

H2SYNC	GENERICC

Provide pull-up pads for these straps - but do not populate. GPIOs functions on these signals must not conflict with the pin strap at Reset

GPIO21_BB_EN



BITLAND Bitland Information Technology Co.,Ltd.
Notebook R&D Division

Title: MINI PCIE SLOT 1,2 (SB)

Size	Document Number	Rev
C	BM5016	1.0

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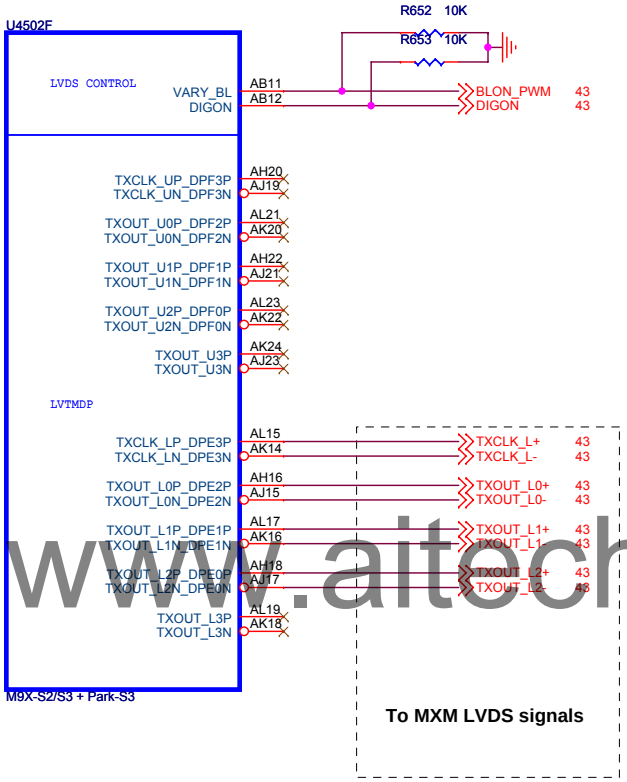
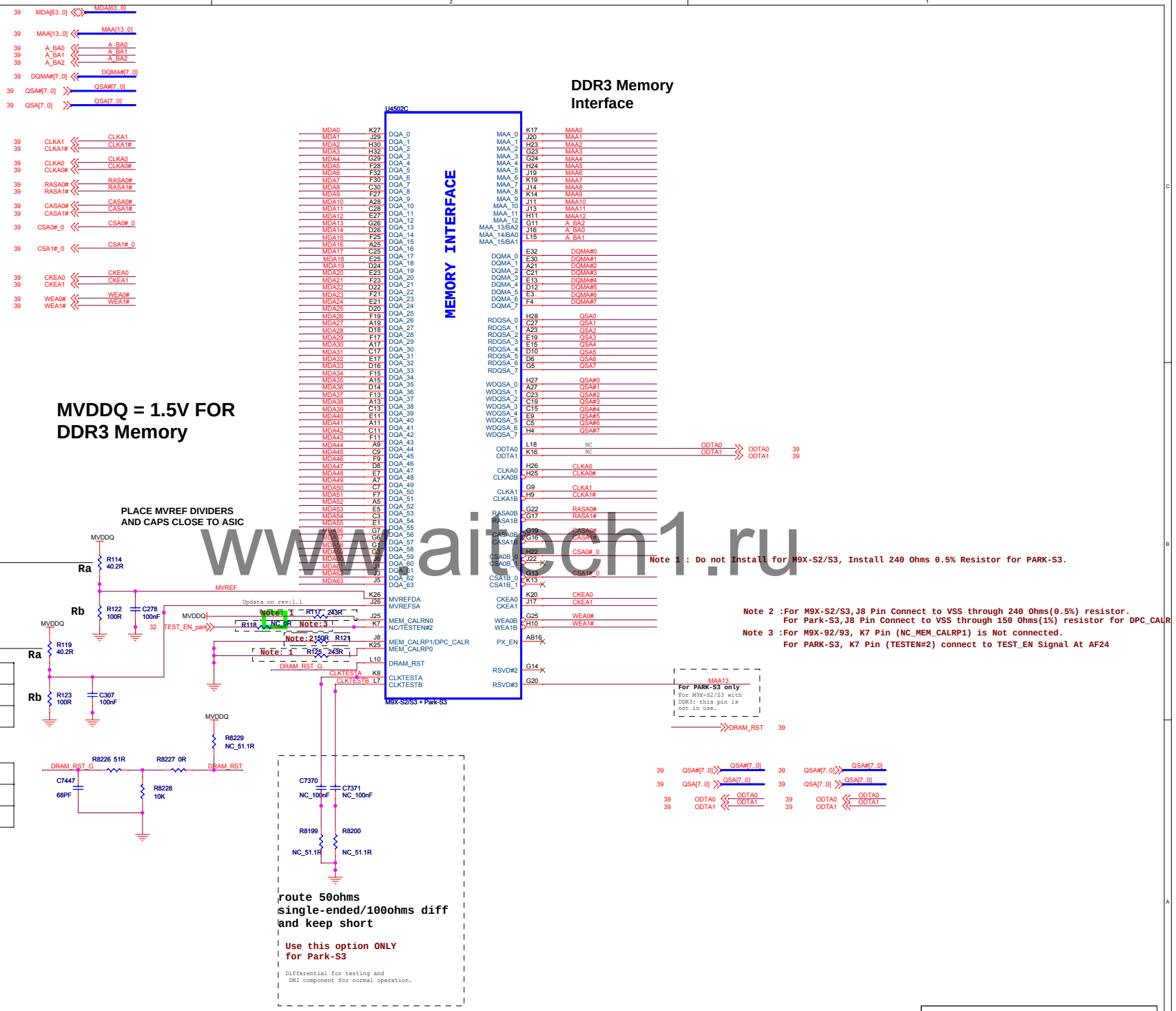
LVDS Interface



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	Park-XT(DPEF_ LVDS)	
Size B	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 37 of 54	

DDR3 Memory Interface



For M9X-S2/S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	100R	40.2R
MVREF TO GND (Rb)	100R	100R

For Park-S3

DIVIDER RESISTORS	DDR2/DDR3	GDDR3
MVREF TO 1.8V (Ra)	40.2R	40.2R
MVREF TO GND (Rb)	100R	100R

BITLAND Bitland Information Techonogy Co.,Ltd. Notebook R&D Division

Title: Park-XT(MEM Interface)

Size: C | Document Number: BM5016 | Rev: 1.0

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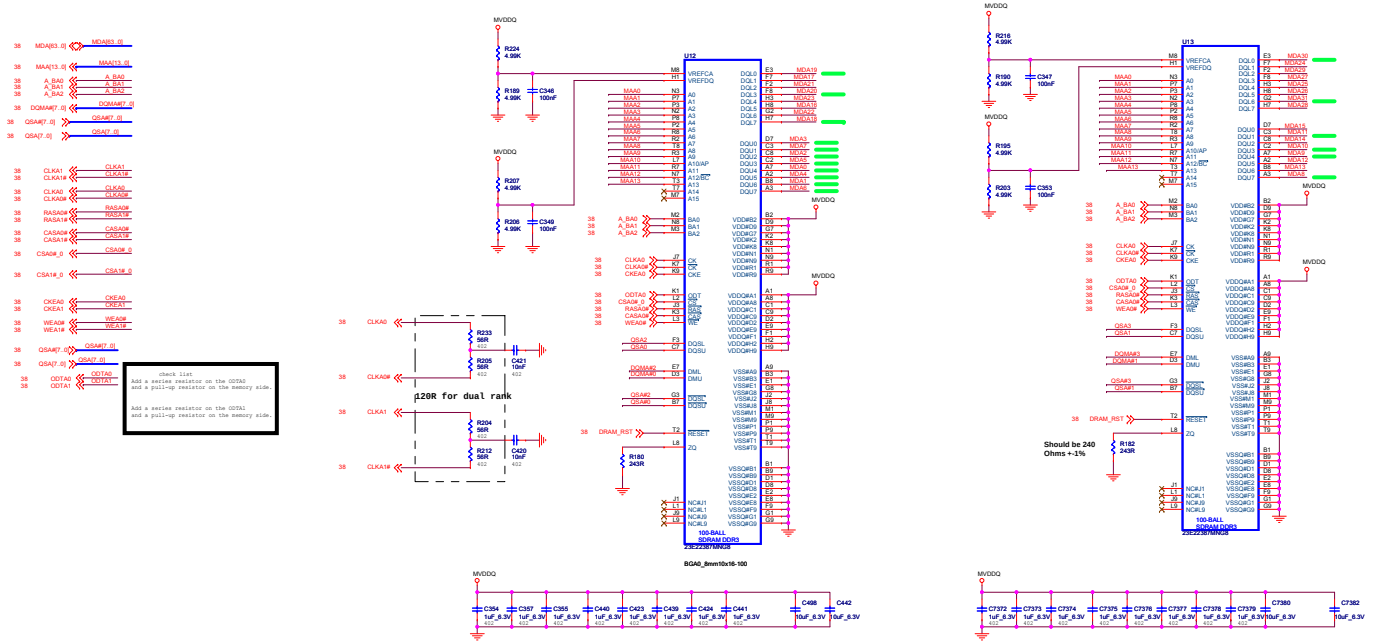
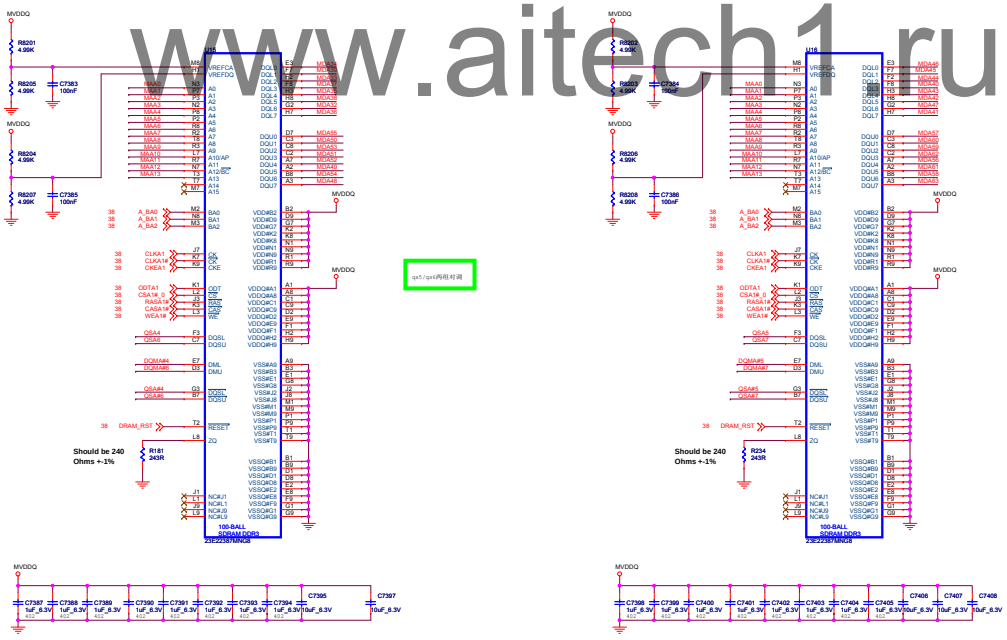


For PARK-S3 with DDR3: Support MAA13-MAA0 Address or 128KX16 DDR3.

RANK1: 256MB/ 512MB DDR3

PARK_XT ENG=750MHZ ,Mem=900MHZ DDR3



COMPONENTS SHOWN ARE EXAMPLES ONLY - AND NOT NECESSARILY QUALIFIED

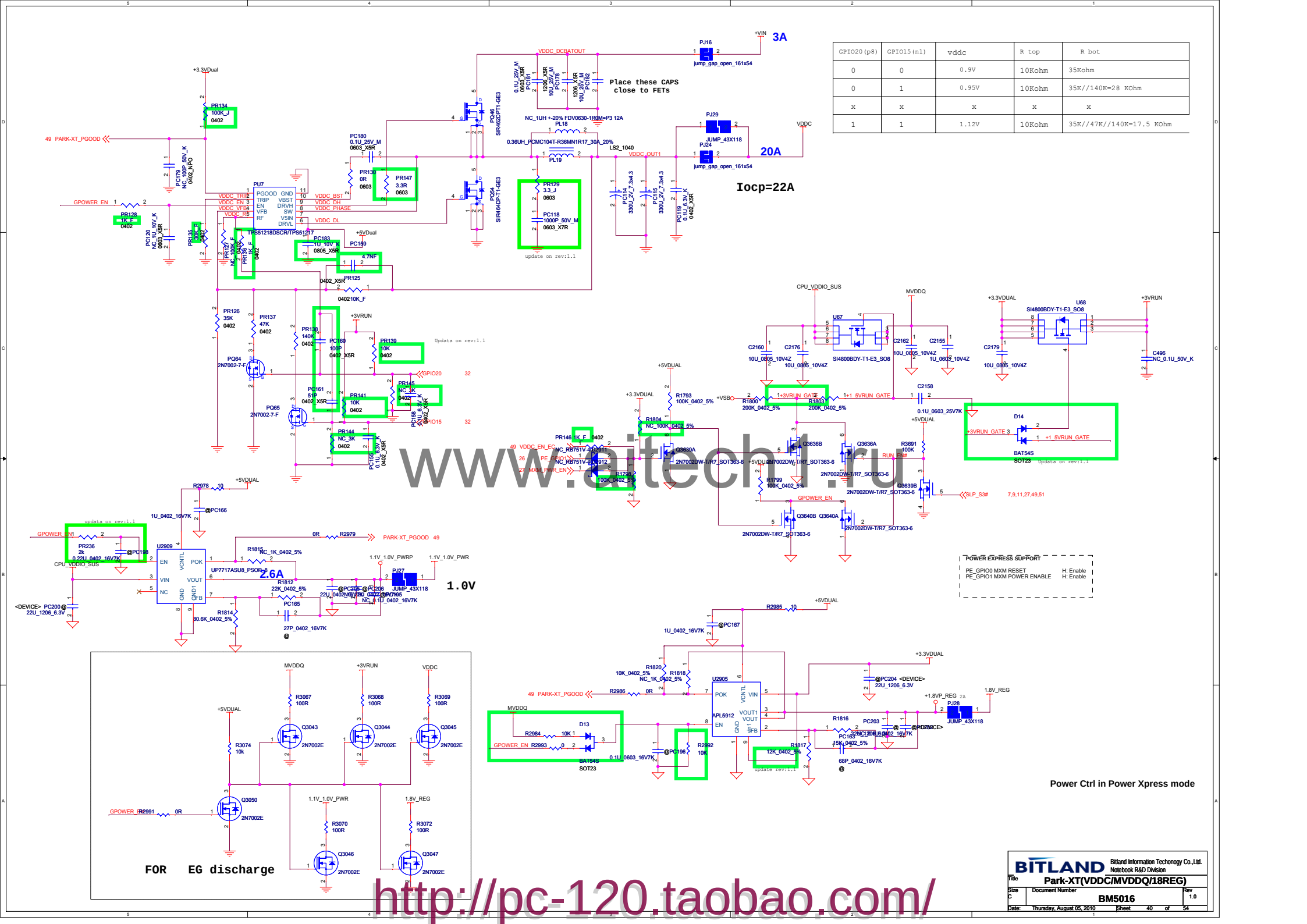
For M9X-S2/S3 with DDR3: Support MAA12-MAA0 Address or 64KX16 DDR3. MAA13 is NC

BITLAND Bitland Information Technology Co.,Ltd. Notebook R&D Division

Title: Park-XT(DDR3 Memory)

Size: D | Document Number: BM5016 | Rev: 1.0

Date: Thursday, August 05, 2010 | Sheet 39 of 54



GPIO20(p8)	GPIO15(n1)	vddc	R top	R bot
0	0	0.9V	10Kohm	35Kohm
0	1	0.95V	10Kohm	35K//140K=28 KOhm
x	x	x	x	x
1	1	1.12V	10Kohm	35K//47K//140K=17.5 KOhm

BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title: Park-XT(VDDC/MVDDQ/18REG)

Size: C | Document Number: BM5016 | Rev: 1.0

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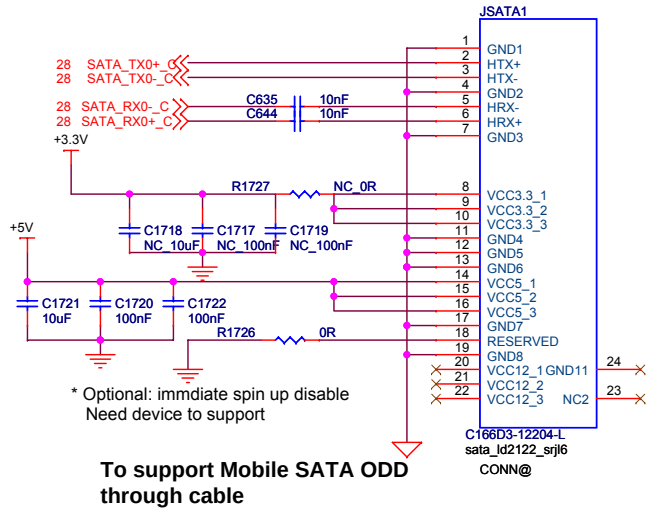
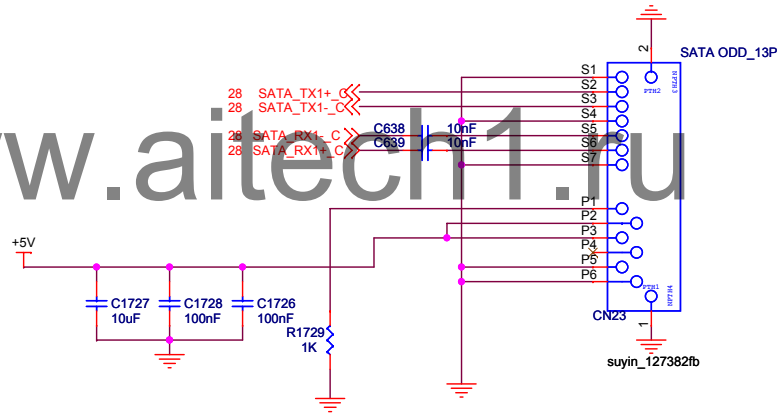
SATA HDD Conn.

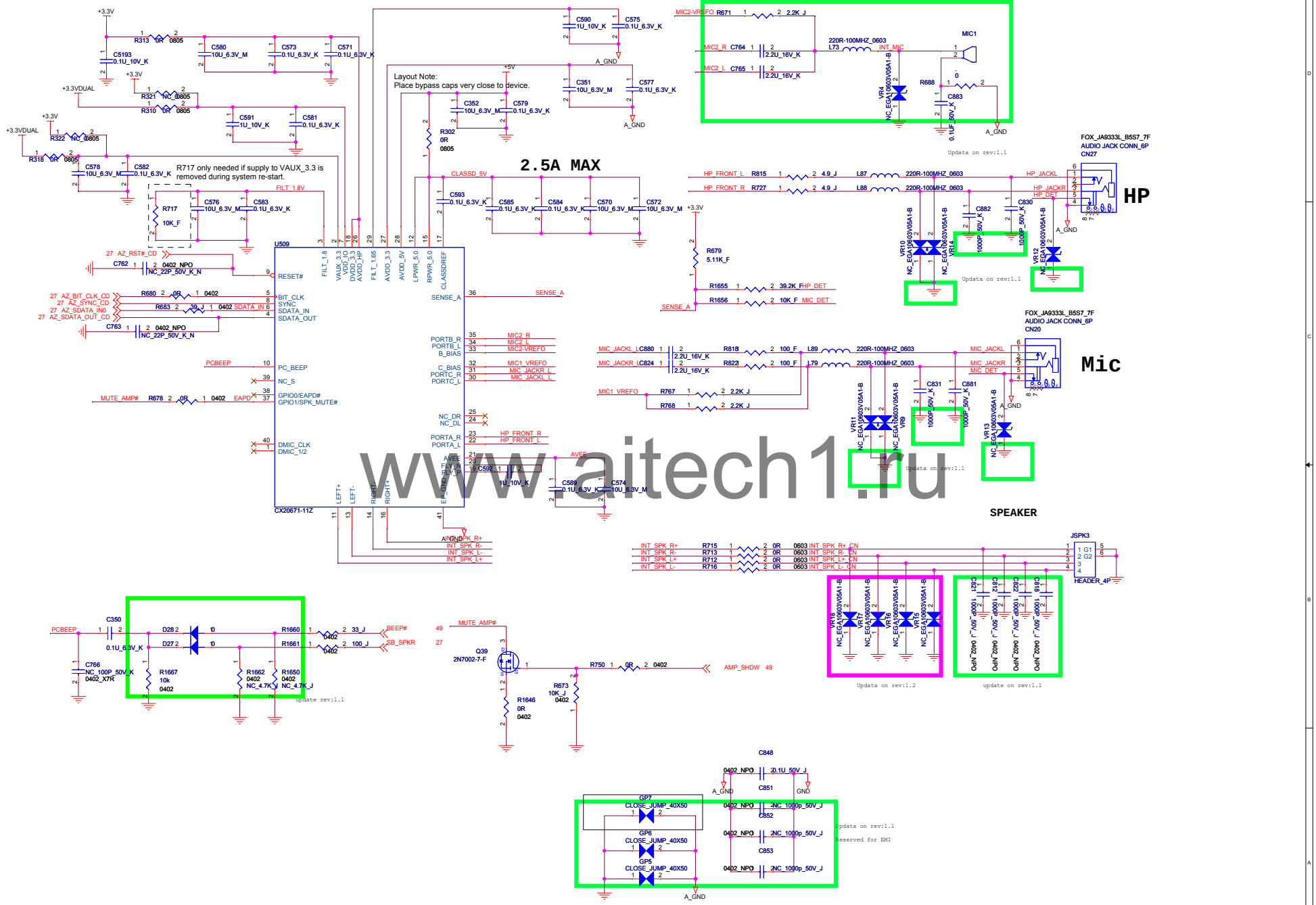


* Optional: immdiate spin up disable
Need device to support

To support Mobile SATA ODD through cable



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	SATA HDD /ODD	
Size B	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 41 of 54	



BITLAND Bitland Information Techonogy Co.,Ltd.
Notebook R&D Division

Title: Audio (CODEC HP MIC)

Size	Document Number	Rev
C	BM5016	1.0

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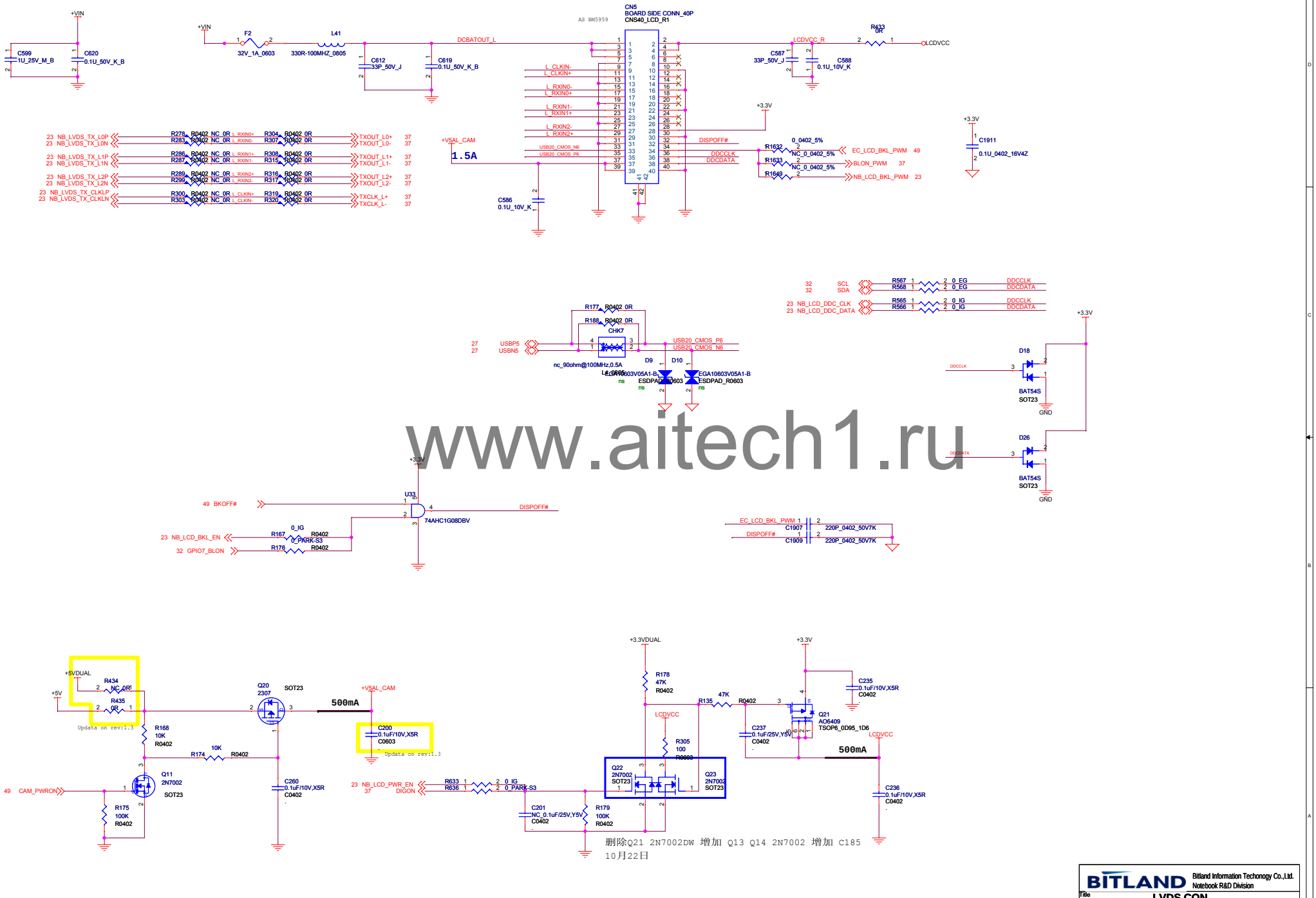
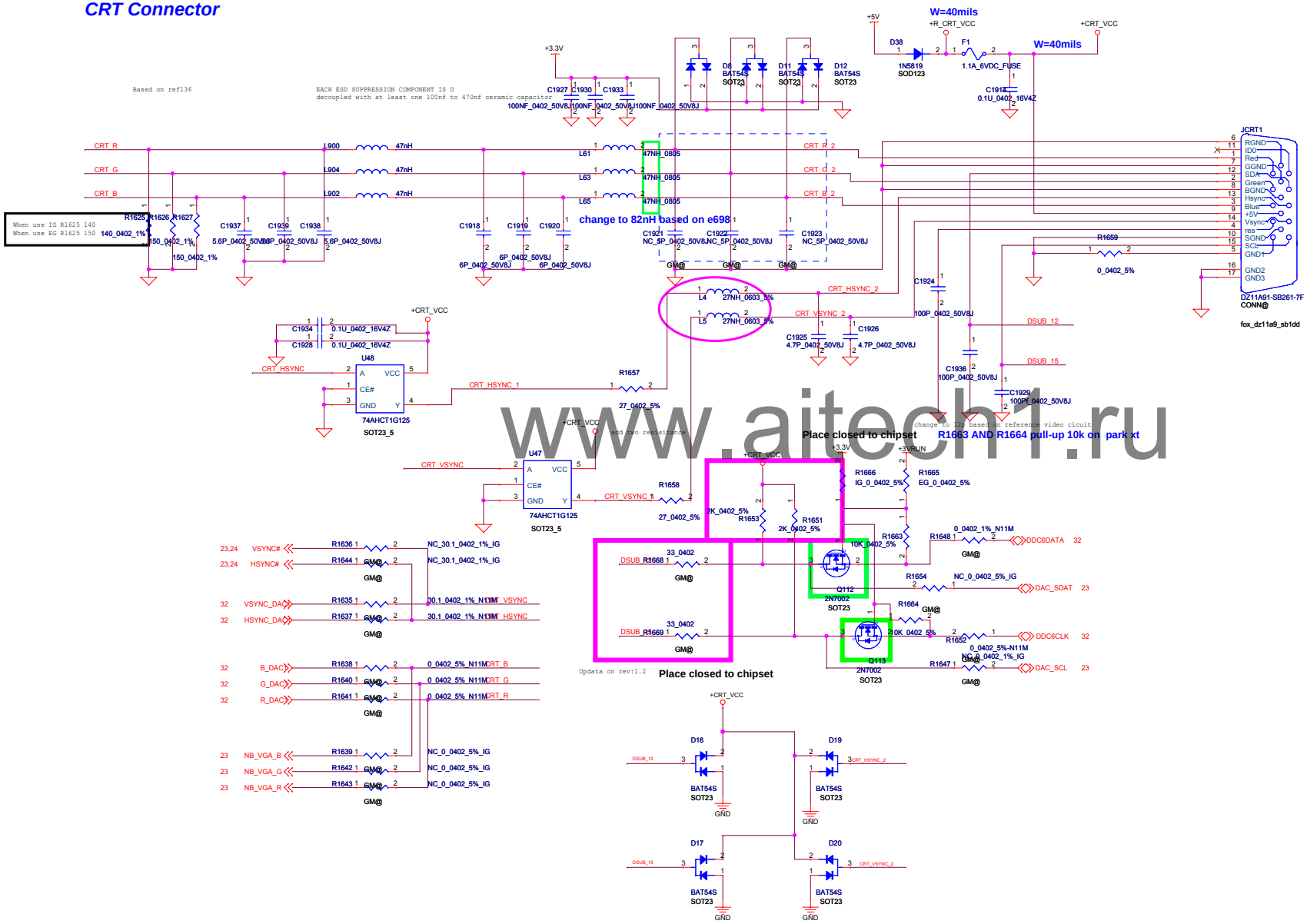
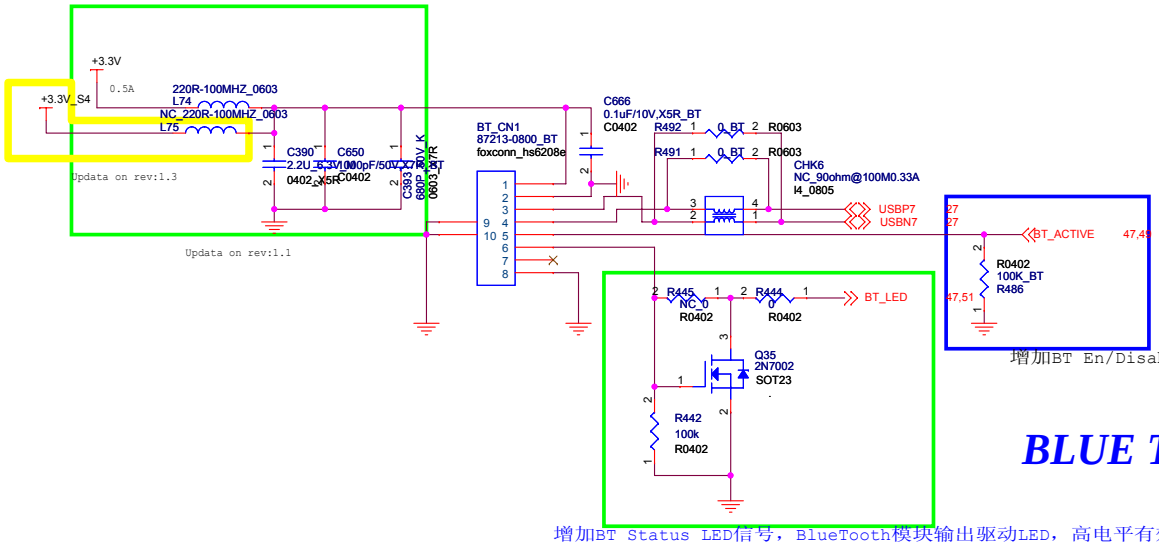


BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	LVDS CON	
Size C	Document Number BM5016	Rev 1.0
Date: Thursday, August 05, 2010	Sheet 43 of 54	

CRT Connector



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title: CRT		
Size: C	Document Number: BM5016	Rev: 1.0
Date: Thursday, August 05, 2010	Sheet 44 of 54	



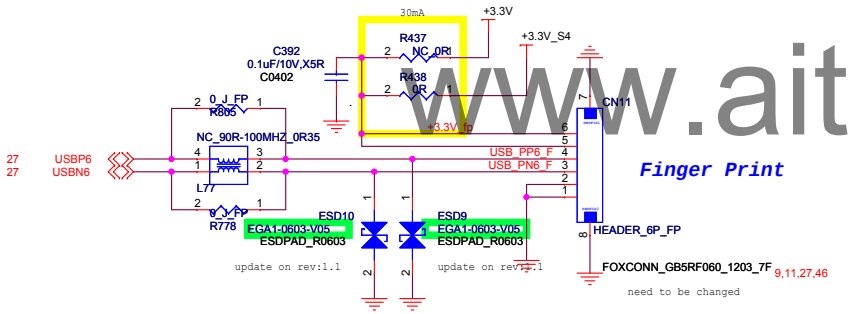
增加BT En/Disable信号，高电平有效。增加对地电阻。

BLUE TOOTH

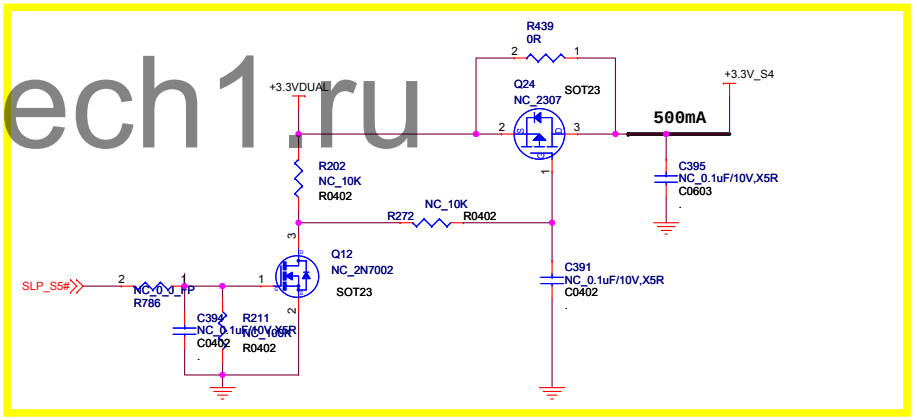
增加BT Status LED信号，BlueTooth模块输出驱动LED，高电平有效

2010-5-20

update on rev:1.1



Finger Print



Updata on rev:1.3

BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	FP / BT / CIR	
Size: Custom	Document Number: BM5016	Rev: 1.0
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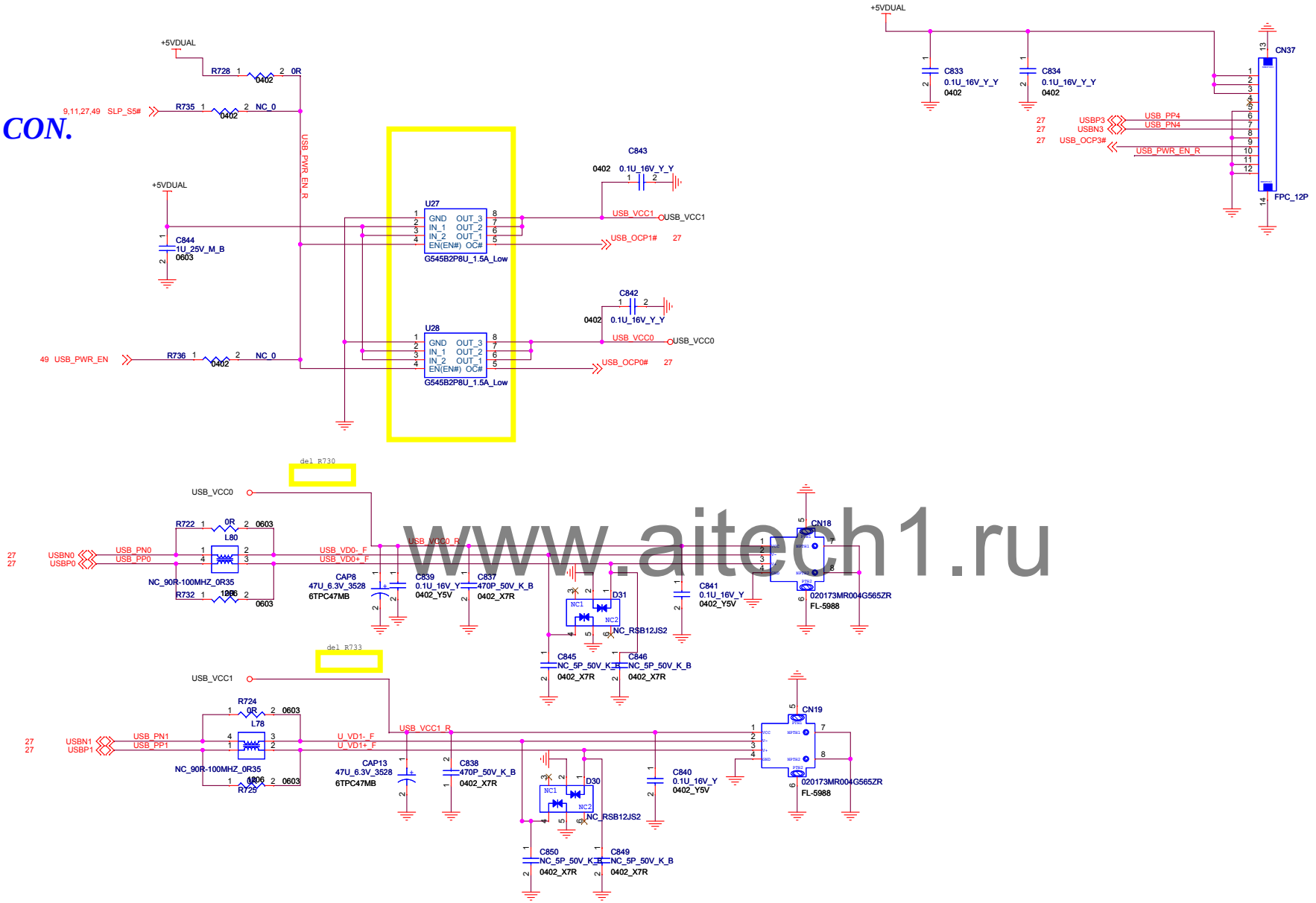
USB CON.



BITLAND	Bitland Information Techonogy Co.,Ltd. Notebook R&D Division	
Title	USB/PW_SW CONN	
Size Custom	Document Number BM5016	Rev 1.0
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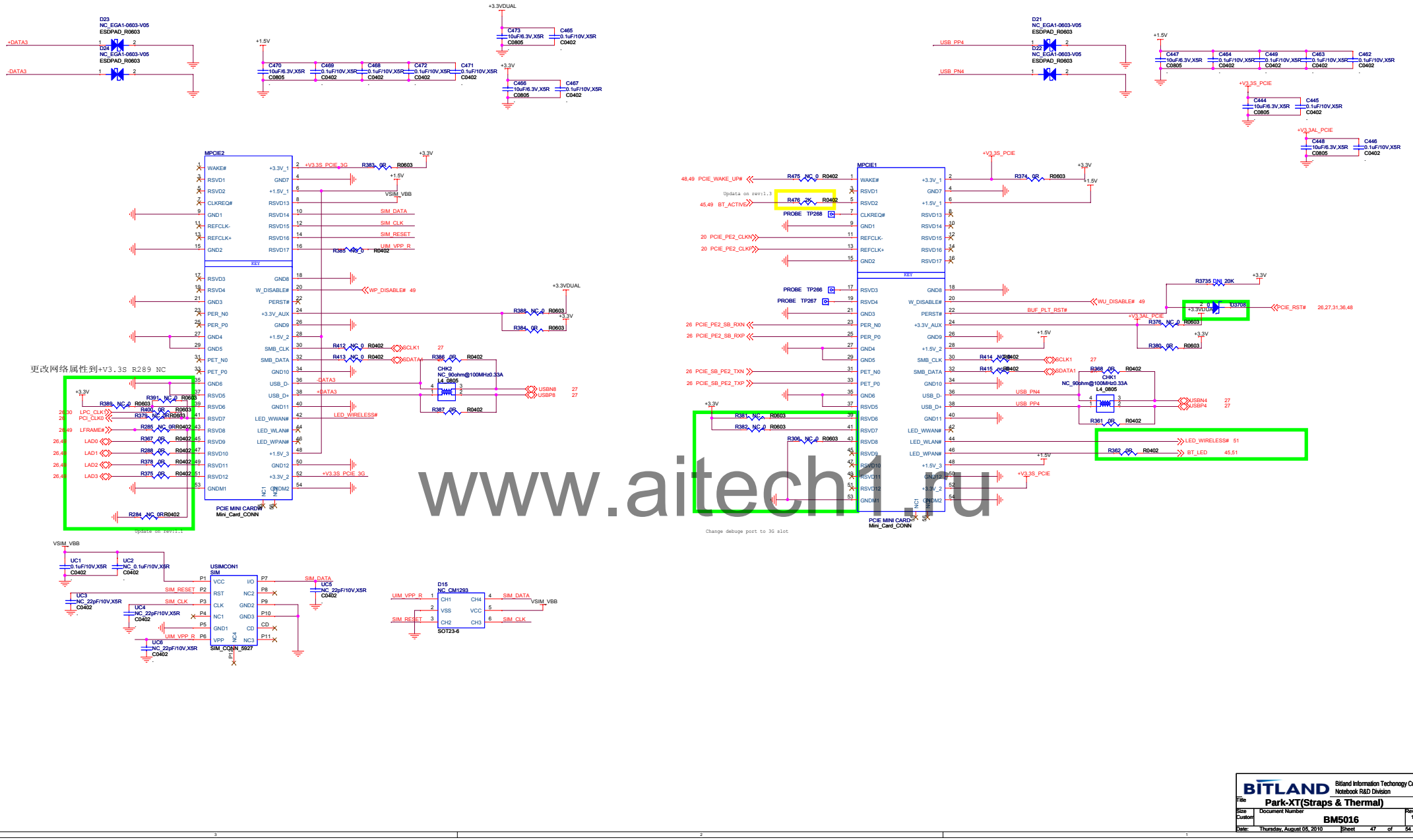

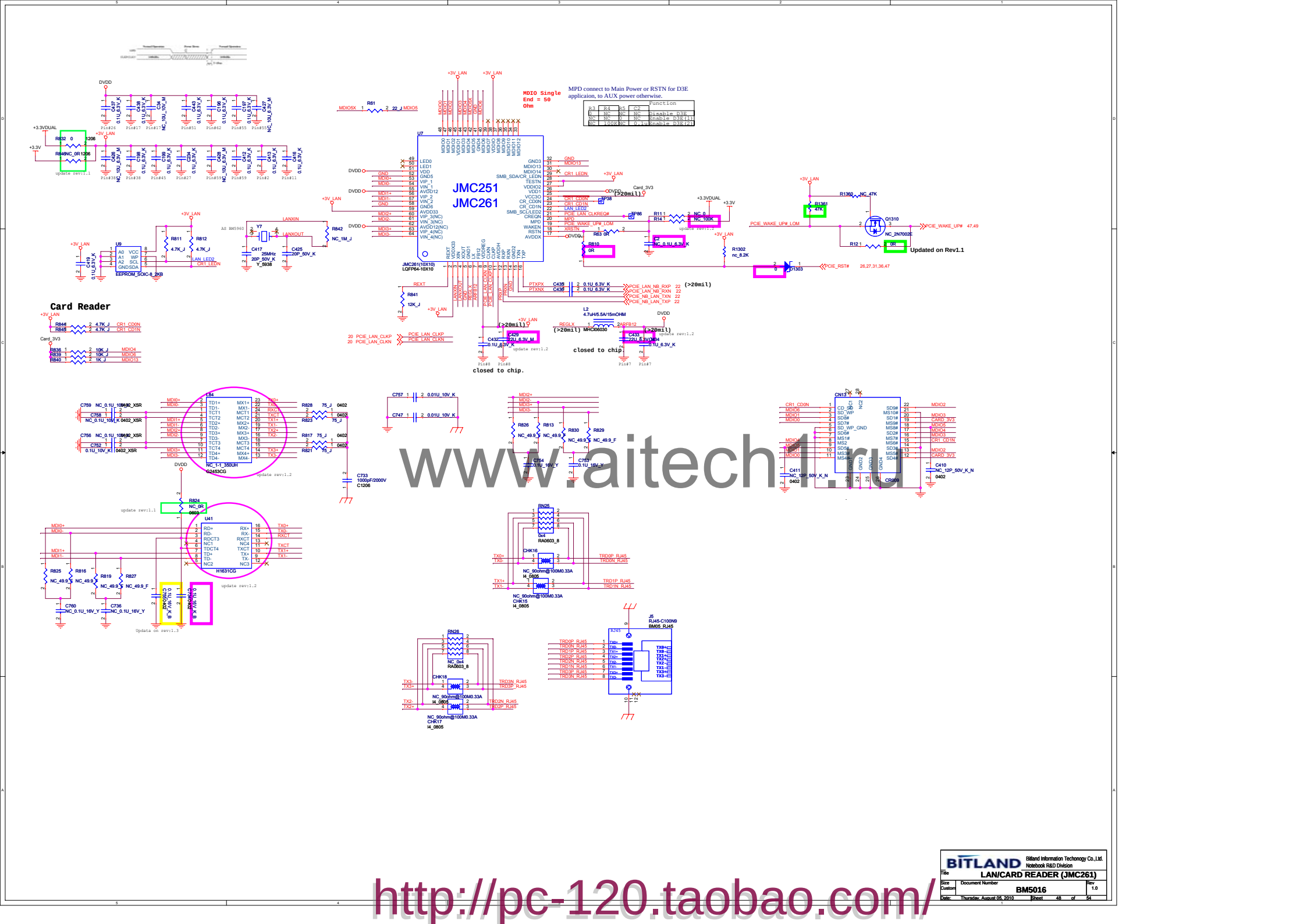
JMC251
JMC261
MDIO Single End = 50 Ohm
MPD connect to Main Power or RSTN for D3E application, to AUX power otherwise.
Function
Disable D3E
Enable D3E(1)
Enable D3E(2)
Updated on Rev1.1
closed to chip.
Card Reader
www.aitech1.ru
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Notebook R&D Division
LAN/CARD READER (JMC261)
BM5016
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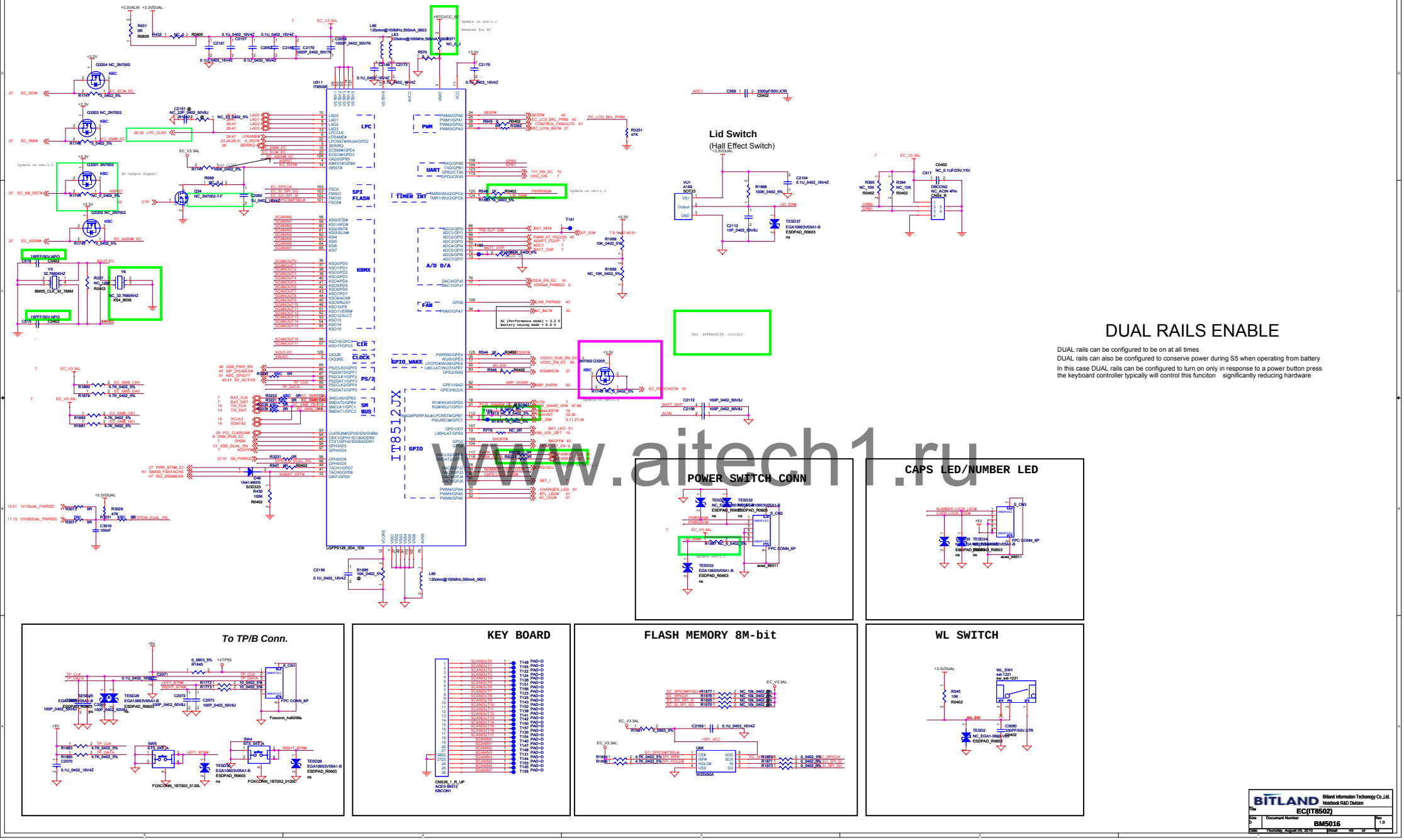
http://pc-120.taobao.com/



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Title	//	
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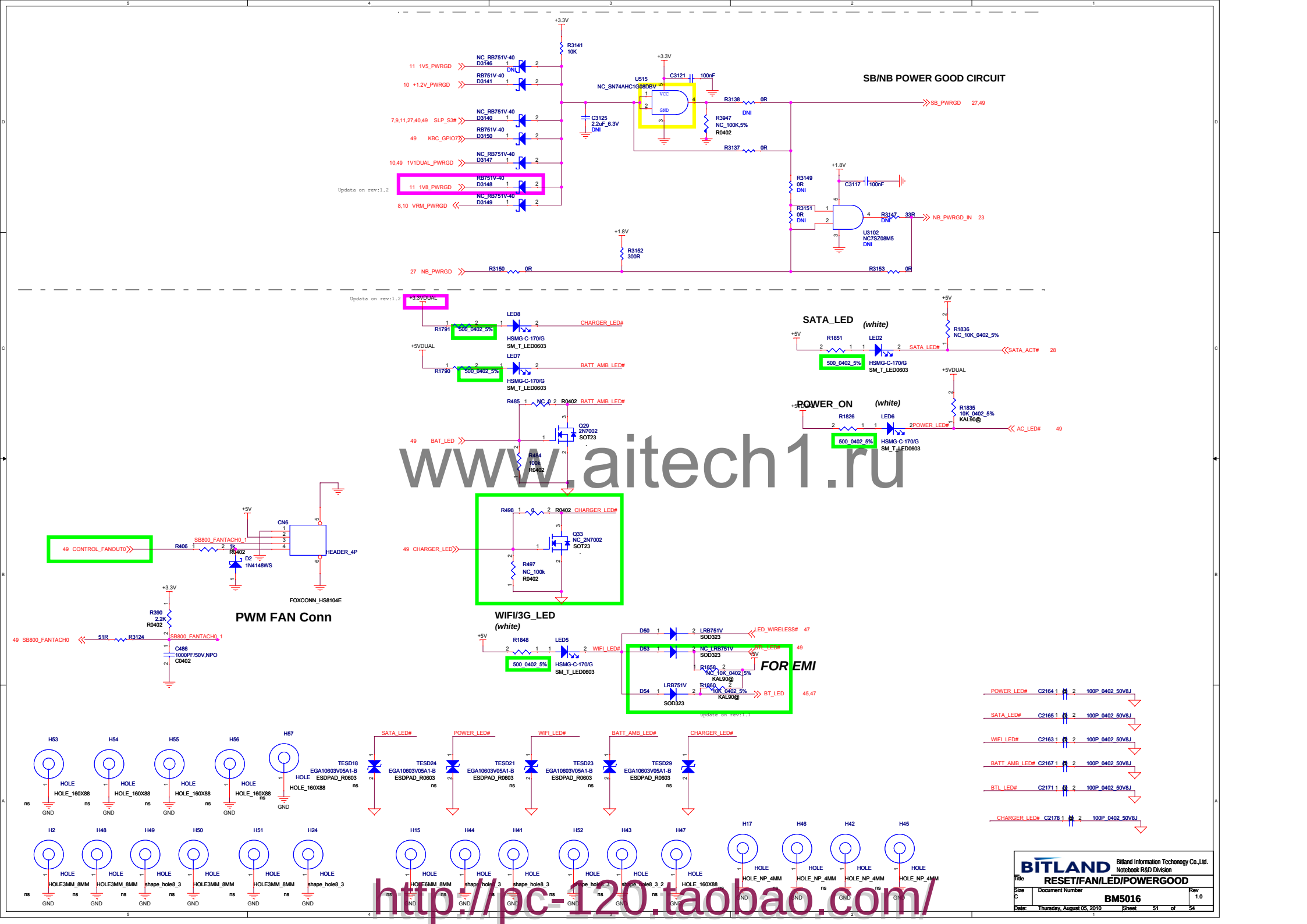
SB/NB POWER GOOD CIRCUIT
SATA_LED (white)
POWER_ON (white)
PWM FAN Conn
WIFI/3G_LED (white)
FOR EMI
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RESET/FAN/LED/POWERGOOD
BM5016
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Title	change history	
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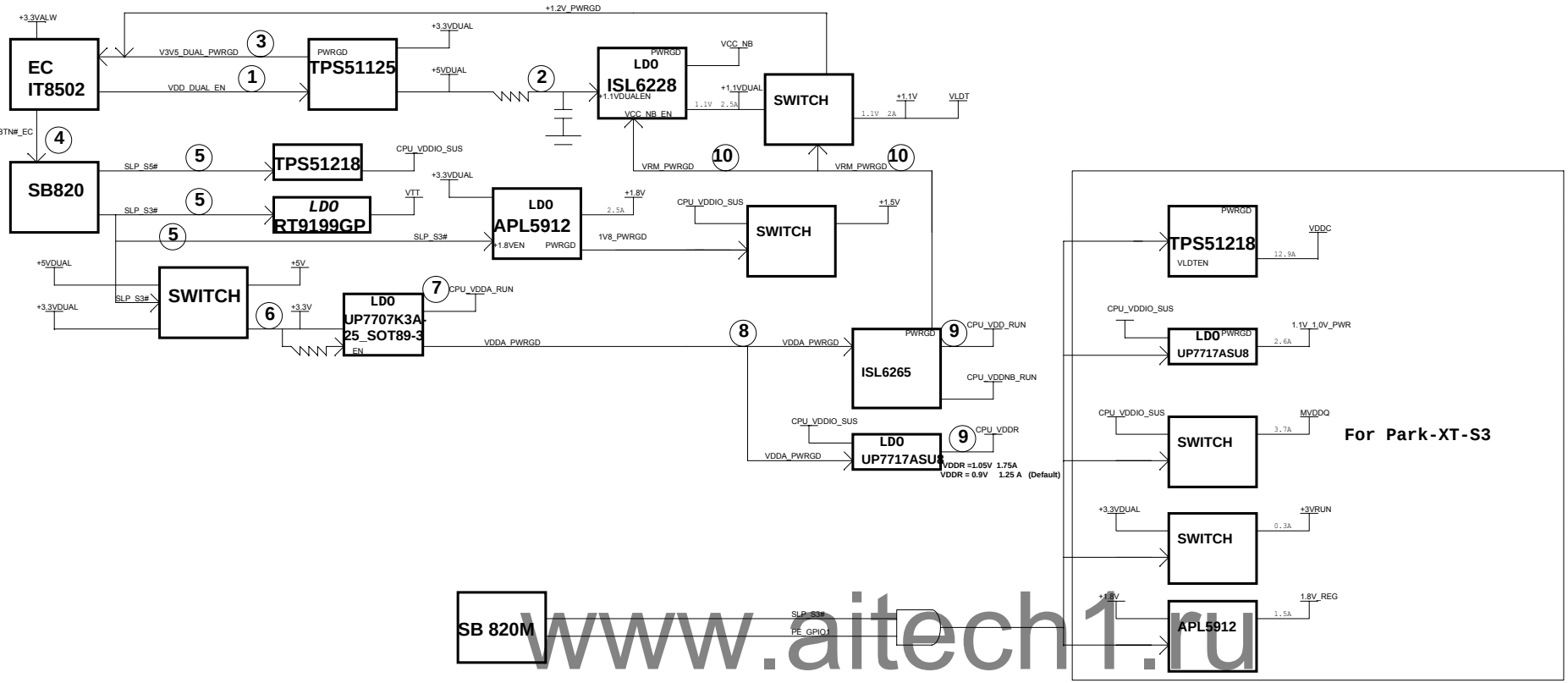

Power on Sequence required:

SB800:

1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:

1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

各电源PWM/L/MOS选型

POWER	PWM	L	H_GATE	L_GATE
+3.3VDUAL (+3.3V 8A)	TI/TPS51125RGER	HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	AO4468 30V 11.6A RDS(ON)<22mΩ(VGS=4.5V)	AO4468 30V 11.6A RDS(ON)<22mΩ(VGS=4.5V)
+5VDUAL (+5V 8A)	VQFN24	HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	AO4468 30V 11.6A RDS(ON)<22mΩ(VGS=4.5V)	AO4468 30V 11.6A RDS(ON)<22mΩ(VGS=4.5V)
VCC_NB (+1.1V 12A)	ISL6228HRTZ-T TQFN-28	HB90109M00LFE 1.0H ±20% 12A 10mΩ SMD-6.6×7.3×3.0mm	VISHAY/SI4172DY-T1-GE3 15A +/-20V 15mΩ@4.5V SO-8pin	VISHAY/SI4168DY-T1-GE3 24A +/-20V 7.6mΩ@4.5V SO-8pin
VLDT (+1.2V 4A)		HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	L/H intergrated (待定)	
VDDIO_SUS (+1.5V 11A)	TPS51218 DSC	HB90109M00LFE 1.0H ±20% 12A 10mΩ SMD-6.6×7.3×3.0mm	VISHAY/SI4172DY-T1-GE3 15A +/-20V 15mΩ@4.5V SO-8pin	VISHAY/SI4168DY-T1-GE3 24A +/-20V 7.6mΩ@4.5V SO-8pin
CPU_VDD_RUN (+1.375~-1.5V 36A)	ISL6265 QFN-48	HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	PHASE1 VISHAY/SiR462DP-T1-GE3 35A +/-20V 0.01Ω@4.5V PowerPAK SO-8pin PHASE2 VISHAY/SiR462DP-T1-GE3 35A +/-20V 0.01Ω@4.5V PowerPAK SO-8pin	VISHAY/SiR466DY-T1-E3/GE3(two) 24.5A +/-20V 6.7mΩ@4.5V SO-8pin VISHAY/SiI466DY-T1-E3/GE3(two) 24.5A +/-20V 6.7mΩ@4.5V SO-8pin
CPU_VDDNB_RUN (0.9V 4A)		HB90479MA0LFE 4.7uH±20% 5.5A 40mΩ SMD-6.86x6.47x3.0mm	L/H intergrated (待定)	
charger	ISL6251HAZ SSOP24_25_150	HB90100MA0LFE 10uH±20% IDC=4A DCR-Max= 71.2mΩ SMD 6.86x6.47x3.0mm	AOS/AON7408 20A RDS(ON)<14mΩ(VGS=4.5V DFN-8)	AOS/AON7702 20A RDS(ON)<14mΩ(VGS=4.5V) DFN-8

LDO

VTT	RT9199GP	(+1.5V---0.75 1.5A)
CPU_VDDA_RUN	APL5508_25DC_TRL SO789_3	(+3.3V---2.5V 500MA)
+1.8V	APL5930	(+3.3V---1.8 1.5A)
CPU_VDDR	APL5912	(+1.5V---1.05V 4A)
+1.1VDUAL	APL5930	(+3.3V---1.1V 500MA)

SWITCH

INPUT(V)	OUTPUT(V)	MOS
+5VDUAL	+5V	AO4468 (8A)
+3.3VDUAL	+3.3V	AO4468 (8A)
VLDT	+1.1V	JUMPER (4A)
CPU_VDDIO_SUS	+1.5V	AO4468 (5A)

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Title: Power sequence

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